CS08/E1
COMMUNICATIONS SUBSYSTEM
TECHNICAL MANUAL

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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The information in this manual is for information purposes and is subject to change without notice.

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TABLE OF CONTENTS

ONE INTRODUCTION

1.1 OVERVIEW 1-1
1.2 RELATED DOCUMENTATION 1-1
1.3 GENERAL DESCRIPTION 1-2
1.4 ORDERING INFORMATION 1-5
1.5 COMPATIBILITY 1-6
1.5.1 Diagnostics 1-6
1.5.2 Hardware and Operating Systems 1-7
1.5.3 Serial Ports 1-7
1.6 FEATURES 1-8

TWO SUBSYSTEM SPECIFICATIONS

2.1 OVERVIEW 2-1
2.2 GENERAL SPECIFICATIONS 2-1
2.3 PHYSICAL SPECIFICATIONS 2-3
2.4 ENVIRONMENTAL SPECIFICATIONS 2-4

THREE INSTALLATION

3.1 OVERVIEW 3-1
3.1.1 Maintaining FCC Class A Compliance 3-1
3.2 INSPECTION 3-1
3.2.1 CC08 Controller Module And Distribution Panel Inspection 3-2
3.3 INSTALLATION OF THE CS08/E1 IN A MicroVAX OR MicroPDP-11 3-3
3.4 INSTALLATION OF THE CS08/E1 IN AN LSI-11 3-5
3.5 CABLING EXTERNAL DEVICES 3-7

FOUR CHOOSING OPTIONS

4.1 OVERVIEW 4-1
4.2 STARTING THE CONFIGURATION PROCESS 4-1
4.3 MAIN MENU 4-2
4.4 CONFIGURATION MENU 4-4
4.4.1 Starting Address 4-4
4.4.2 Starting Vector 4-5
4.4.3 Bus Request Level 4-5
4.4.4 Enable Emulex Options 4-5
4.4.5 Force Two Stop Bits 4-6
4.4.6 User Defined Baud Rate 4-6
4.4.7 Break Timing 4-7
4.4.8 Level Flow Control 4-7

FIVE OPERATION

5.1 OVERVIEW 5-1
5.2 DIAGNOSTICS 5-1
5.3 OPERATING SYSTEMS 5-2
5.3.1 Bus and Vector Addresses 5-2
5.3.2 Adding A New Device To RSTS/E 5-2
5.3.2.1 Generating A New Monitor With SYSGEN 5-3
5.3.2.2 Assigning Bus And Vector Addresses 5-3
5.3.2.3 Modem Controls 5-4
5.3.3 Adding A New Device To RSX-11M 5-5
5.3.3.1 Modem Controls 5-6
5.3.4 Adding A New Device To RSX-11M-PLUS 5-7
5.3.4.1 Modem Controls 5-8
5.3.5 Adding A New Device To Ultrix-11 5-9
5.3.5.1 Enabling Terminals And Modem Controls 5-9
5.3.6 Adding A New Device To MicroVMS 5-11
5.3.6.1 Modem Controls 5-12
5.3.7 Adding A New Device To Ultrix-32m 5-13
5.3.7.1 Enabling Terminals And Modem Controls 5-13

SIX TROUBLESHOOTING

6.1 OVERVIEW 6-1
6.1.1 Service 6-1
6.1.2 Test Connector 6-2
6.2 FAULT ISOLATION PROCEDURES 6-2
6.3 POWER-UP SELF TESTS 6-4
6.3.1 CC08 Controller Module Self-Test 6-4

SEVEN DEVICE REGISTERS AND PROGRAMMING

7.1 OVERVIEW 7-1
7.2 DHV11 REGISTER 7-1
7.2.1 Control Status Register (CSR) 7-3
7.2.2 Receiver Buffer (RBUF) 7-5
7.2.3 Transmit Character Buffer (TXCHAR) 7-7
7.2.4 Line Parameter Register (LPR) 7-8
7.2.5 Line Status (STAT) 7-11
7.2.6 Line Control (LNCTRL) 7-12
7.2.7 Transmit Buffer Address 1 (TBUFFAD1) 7-16
7.2.8 Transmit Buffer Address 2 (TBUFFAD2) 7-16
7.2.9 Transmit DMA Buffer Counter (TBUFFCT) 7-17
7.3 DHV11 GENERAL PROGRAMMING INFORMATION 7-18
7.3.1 Initialize 7-18
7.3.2 Programmable Parameters 7-19
7.3.3 Interrupts 7-19
7.3.4 Data Flow Control 7-20
7.3.5 Diagnostic Codes 7-21
7.3.5.1 Self-Test Diagnostic Codes 7-21

7.3.5.2	Interpretation of Self-Test Codes	7-21
7.3.5.3	Skipping Self-Test	7-23
7.3.6	Error Indication	7-23
7.3.7	Background Monitor Program	7-24
7.3.8	Receiver Operation	7-24
7.3.8.1	Receiver Scanner	7-24
7.3.8.2	FIFO Buffer Operation	7-24
7.3.8.3	Half-Duplex Operation	7-24
7.3.9	Transmitter Operation	7-25
7.3.9.1	DMA Transmission	7-25
7.3.9.2	Single Character Transmission	7-25
7.3.9.3	Modem Control	7-26
7.4	CC08 CONTROLLER ARCHITECTURE	7-27
7.4.1	Receiver Operation	7-28
7.4.2	Transmitter Operation	7-28

A CABLE SCHEMATICS

B ASSIGNING BUS AND VECTOR ADDRESSES

B.1	OVERVIEW	B-1
B.2	CALCULATING BUS AND VECTOR ADDRESSES	B-2
B.2.1	Using the MicroVMS CONFIGURE Command	B-2
B.2.2	Calculating the Bus Address	B-4
B.2.2	Calculating the Interrupt Vector Address Manually	B-6
B.2.3	System Configuration Worksheet	B-9
B.2.4	A System Configuration Example	B-12

C DHV11 DIAGNOSTIC

C.1	GENERAL DESCRIPTION	C-1
C.2	DIAGNOSTIC TEST FUNCTIONS	C-2
C.2.1	Diagnostic Exceptions	C-3
C.3	DIAGNOSTIC SUPERVISOR SUMMARY	C-3
C.4	LOADING PROCEDURES	C-3
C.5	STARTING THE DIAGNSTIC PROGRAM	C-4
C.6	DRS SUPERVISOR COMMANDS	C-6
C.6.1	Command Switches	C-6
C.6.2	Control/Escape Characters Supported	C-8
C.7	DHV11 DIAGNOSTIC EXAMPLE	C-8

D PROM REMOVAL AND REPLACEMENT

E ASCII CODE CONVERSION

LIST OF TABLES

1-1	CS08/E1 Standard Components	1-5
1-2	CS08/E1 Optional Accessories	1-6
1-3	Serial Port Pin/Signal Assignments	1-7
2-1	CS08/E1 General Specification	2-1
2-2	CC08 Controller Module Physical Specification	2-3
2-3	CC08 Controller Module Environmental Specification	2-4
4-1	Timer Count/Baud Rate Translation	4-6
7-1	Transmit and Receive Data Rates for the DHV11	7-9
7-2	Default Line and Register Values	7-18
7-3	DHV11 Self-Test Diagnostic Codes	7-22
7-4	DHV11 Self-Test Error Codes	7-22
A-1	SYSGEN Device Table	B-5
A-2	Priority Ranking for Floating Vector Addresses	B-7
A-3	Floating Address Computation	B-12
A-4	Interrupt Vector Address Example	B-13

LIST OF FIGURES

1-1	CS08/E1 Physical Layout	1-2
1-2	CC08 Controller Module and CP08/M Distribution Panel	1-3
1-3	CC08 Controller Module and CP08/J Distribution Panel	1-4
2-1	CC08 Controller Module Dimensions	2-3
3-1	MicroPDP/VAX Patch Panel Assembly	3-3
3-2	Typical Completed MicroVAX Installation (CP08/M)	3-4
3-3	Typical Completed MicroVAX Installation (CP08/J)	3-5
3-4	Typical Completed LSI-11 Installation (CP08/M)	3-6
3-5	Typical Completed LSI-11 Installation (CP08/J)	3-7
4-1	Main Menu	4-2
4-2	Configuration Menu	4-4
7-1	DHV11 Registers	7-2
7-2	CC08 Controller Module Block Diagram	7-27
A-1	Terminal Cable (25-Pin to 25-Pin)	A-2
A-2	Terminal Cable (RJ11 to RJ11)	A-2
A-3	RJ11 to DB25S	A-3
A-4	Modem Cable	A-3
A-5	Null-Modem Cable	A-4
A-6	Terminal Cable for Ports Using Level Flow Control	A-4
A-7	Wraparound CP08/M	A-5
A-8	Wraparound CP08/J	A-5
A-9	Staggered Loopback CP08/M	A-6
A-10	Staggered Loopback CP08/J	A-6
B-1	Sample SHOW CONFIGURATION	B-3
B-2	CONFIGURE Command Listing	B-4
B-3	Bus Address Worksheet	B-11
C-1	Staggered Loopback Cable Configuration	C-2
D-1	Location of CS08/E1 Emulation PROMs on PCBA	D-2

EMULEX PRODUCT WARRANTY

CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex controller product supplied shall be free from defects in material and workmanship.

CABLE WARRANTY: All Emulex provided cables are warranted for ninety (90) days from the time of shipment.

The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors, adaptors, and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the product, or use of the product is such a manner for which it was not designed, or by causes external to the product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace any defective product, and, unless otherwise stated, pay return transportation cost for such replacement. Purchaser shall provide labor for removal of the defective product, shipping charges for return to Emulex and installation of its replacement.

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RETURNED MATERIAL: Warranty claims must be received by Emulex within the applicable warranty period. A replaced product, or part thereof, shall become the property of Emulex and shall be returned to Emulex at Purchaser's expense. All returned material must be accompanied by a RETURN MATERIALS AUTHORIZATION (RMA) number assigned by Emulex.

Section 1
INTRODUCTION

1.1 Overview

This manual describes the Emulex CS08/E1, an 8-line communications subsystem that emulates Digital Equipment Corporation's DHV11 asynchronous multiplexer.

This manual contains both installation and programming information, as follows:

- **Section 1 (Introduction)** is the section you are reading now.
- **Section 2 (Specifications)** contains detailed general, physical, and environmental specifications for the CS08/E1.
- **Section 3 (Installation)** describes the physical installation of the CS08/E1.
- **Section 4 (Options)** describes how to select subsystem options.
- **Section 5 (Operation)** describes how to run diagnostics and configure the operating system.
- **Section 6 (Troubleshooting)** describes fault isolation procedures.

In addition, Section 7 (Programming) describes the controller's DHV11-type registers and provides a brief description of the controller architecture.

Several appendices provide miscellaneous diagnostic, cabling, and operating system information.

1.2 Related Documentation

This manual is the main piece of documentation for the CS08/E1. Two other manuals are also included with the subsystem:

- **Distribution Panel Technical Manual.** This manual describes how to set up and install the distribution panel.
- **Diagnostic User's Guide (optional).** This manual describes how to run the CS08/E1 MicroVAX diagnostics. It is included only if MicroVAX diagnostics are ordered.

In general, these manuals are needed only during specific parts of the installation. This manual will clearly reference them whenever you need them.

1.3 General Description

The CS08/E1 is a communications subsystem that provides up to eight asynchronous serial lines and emulates the DEC DHV11 asynchronous multiplexers.

There are two versions of the CS08/E1 subsystem, one with and one without modem support. Each consists of two parts:

- The CC08 Controller, packaged on a dual-wide board, plugs directly into any Q-Bus backplane slot. It emulates one DHV11 and is compatible with any Q-Bus system, including the LSI-11 series, the MicroPDP-11, and the MicroVAX I and II.

- The CP08 Distribution Panel connects to the CC08 Controller and contains the subsystem's serial ports. The CP08 is available in two versions: the CP08/M contains eight RS-232 serial ports and supports six modem signals on each port, using 25-pin connectors on a double size B board. The CP08/J contains eight RS-232 serial ports using RJ12 connectors on a single size B board. It does not support modem signals.

  Either CP08 is designed to mount directly in the rear bulkhead of a MicroPDP-11 or MicroVAX. With a special mounting adapter and cables, either can also be mounted in a standard 19-inch RETMA equipment rack.

Figure 1-1 illustrates the basic setup of the CS08/E1 in a typical system. Figure 1-2 is a photograph of the CC08 Controller Module and the CP08/M Distribution Panel. Figure 1-3 is a photograph of the CC08 Controller Module and the CP08/J Distribution Panel.

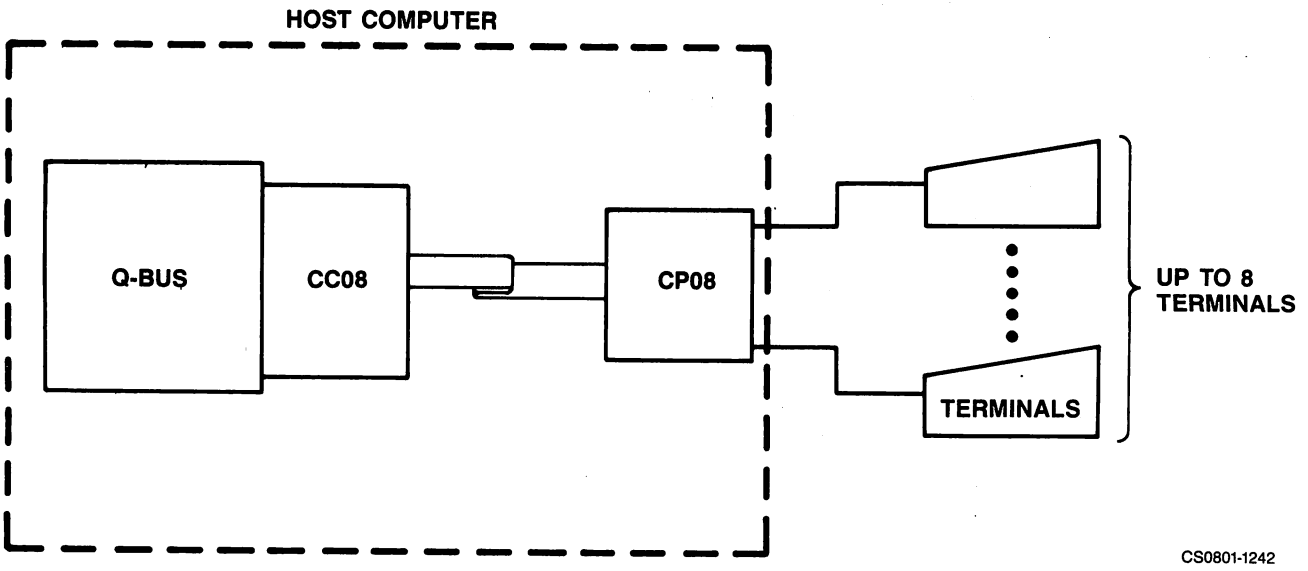

Figure 1-1. CS08/E1 Physical Layout

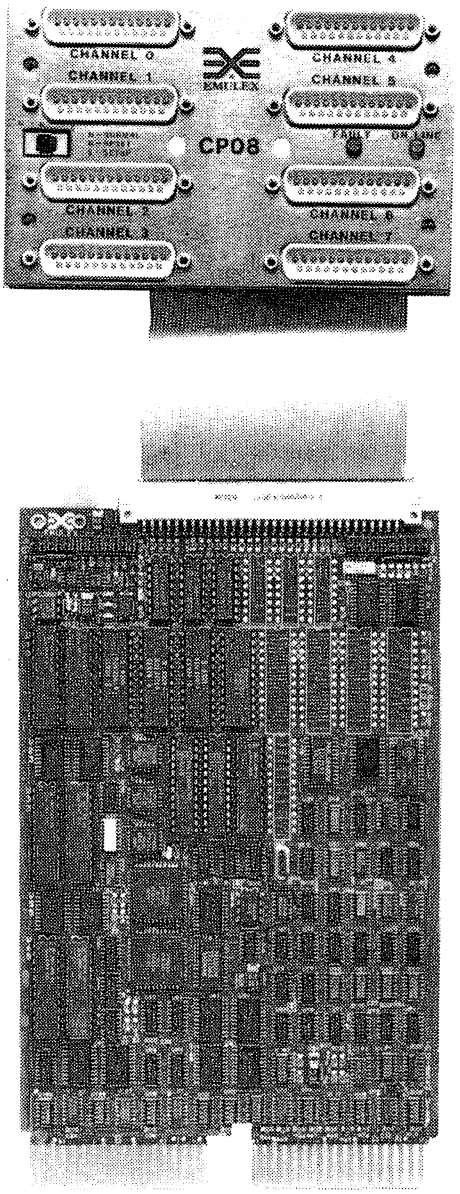

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Figure 1-2. CC08 Controller Module and CP08/M Distribution Panel

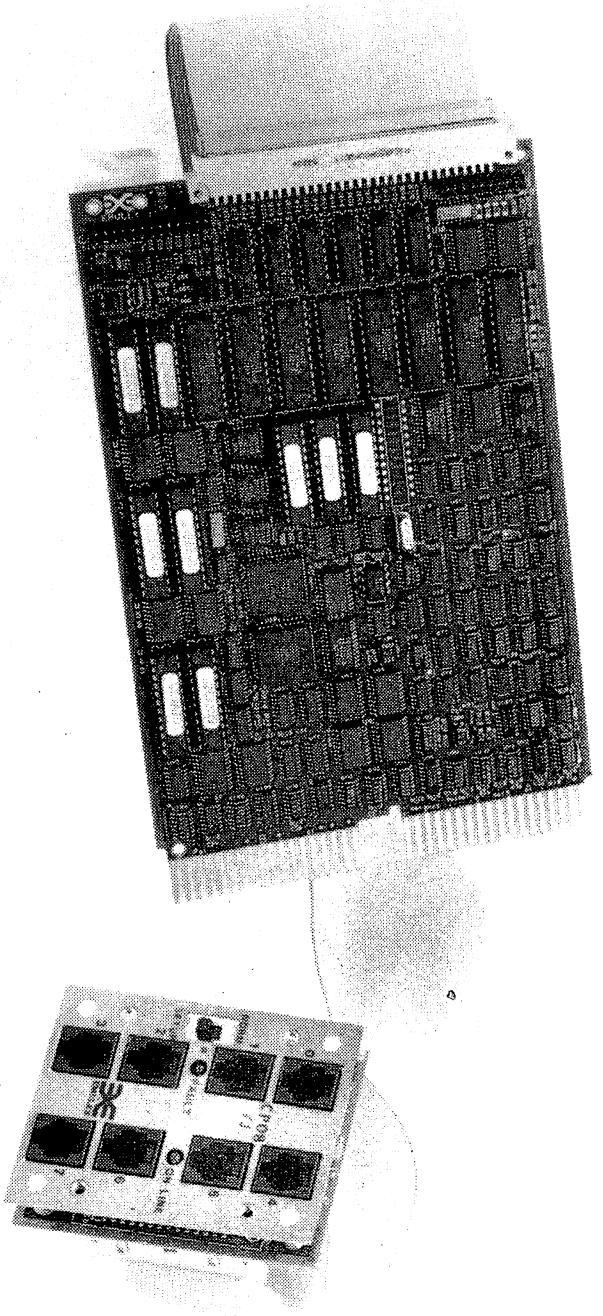

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Figure 1-3. CC08 Controller Module and CP08/J Distribution Panel

1.4 Ordering Information

All versions of the CS08/E1 come with the components listed in Table 1-1. In addition, several optional accessories are available, such as different lengths of cables, mounting brackets, etc. These options are listed in Table 1-2.

Table 1-1. CS08/E1 Standard Components

Item	Description	Part Number	Comment
1	CC08 Controller	CS0810201-00	
2	CP08 Distribution Panel		
	CP08/M	CP0810201-00	25 pin connector
	CP08/J	CP0810202-00	RJ12 connector
3	64-Wire Ribbon Cable		
	1.5 foot	CU0911201-01	Connects controller to CP08/M
	1.5 foot	CU0811201-01	Connects controller to CP08/J
4	CS08/E1 Technical Manual	CS0851001-00	
5	Distribution Panel Technical Manual		
	CP08/M	CP0851001-00	
	CP08/J	CP0851002-00	

Table 1-2. CS08/E1 Optional Accessories

Item	Description	Part Number	Comment
1	64-Wire Ribbon Cable		
	4 foot	CU0911201-02	Connects controller to CP08/M
	8 foot	CU0911201-03	Connects controller to CP08/M
	4 foot	CU0811201-02	Connects controller to CP08/J
	8 foot	CU0811201-03	Connects controller to CP08/J
2	Rack-Mount Chassis	CU2213002-00	Required if CP08/M or CP08/J is rack-mounted
3	Rack-Mount Adapter		
	CP08/M	CP0920602-00	Required if CP08/M is rack-mounted or installed in DEC I/O connection panel
	CP08/J	CP0810204-00	Required if CP08/J is rack-mounted or installed in DEC I/O connection panel
4	Wraparound Connector	CU2210202-00	For diagnostic use with CP08/M
5	Staggered Loopback Cable		
	CP08/M	CU0411202-00	For diagnostic use
	CP08/J	5300507	For diagnostic use
6	Diagnostics		
	for LSI-11	PX9951801-xx	
	for MicroVAX	VX9951804-xx	

1.5 Compatibility

This section describes the software and hardware requirements of the CS08/E1 subsystem.

1.5.1 Diagnostics

On LSI-11 CPUs, the CS08/E1 executes the following DEC diagnostics:

- CVDHA??
- CVDHB??
- CVDHC??

The notation "??" represents the version level and patch level of the diagnostic. Instructions for running these diagnostics are contained in Appendix C.

On the MicroVAX I and II, Emulex supplies its own diagnostic, IQC09E. An instruction manual for running the diagnostic is included with the diagnostic media.

Both the LSI-11 diagnostics and the MicroVAX diagnostics are optionally available from Emulex (see Table 1-2 for part numbers).

1.5.2 Hardware and Operating Systems

The CS08/E1 is electrically and mechanically compatible with all Q-Bus applications and with all DEC operating systems that support the DHV11.

1.5.3 Serial Ports

The serial ports on either CP08 Distribution Panel are electrically compatible with the RS-232-C standard. Physically, the ports on the CP08/M use a 25-pin connector, and the ports on the CP08/J use an RJ12 connector.

The CP08/M supports all modem control signals supported by the DEC DHV11. Table 1-3 shows the signals supported by the CP08 distribution panels.

Table 1-3. Serial Port Pin/Signal Assignments

Function	DHV11	CP08/M		CP08/J	
	Support	Support	Pin #	Support	Pin #
Chassis Ground	Yes	Yes	1	No	
Transmit Data	Yes	Yes	2	Yes	2
Receive Data	Yes	Yes	3	Yes	5
Request To Send	Yes	Yes	4	No	
Clear To Send	Yes	Yes	5	No	
Data Set Ready	Yes	Yes	6	No	
Signal Ground	Yes	Yes	7	Yes	3,4
Carrier Detect	Yes	Yes	8	No	
Data Terminal Ready	Yes	Yes	20	No	
Ring	Yes	Yes	22	No	

1.6 Features

The CS08/E1 contains several advanced features:

- **Small size.** The CC08 Controller Module is packaged on a dual size board. Thus, it takes up half the backplane space of the equivalent DEC controllers.
- **Ease of configuration.** There are no switches to set on the CS08/E1. All options are chosen after the installation is complete by attaching a terminal to the distribution panel and stepping through a simple, menu-driven configuration program.
- **Full modem controls.** Full modem controls are available on all eight channels with the CP08/M Distribution Panel.
- **Programmable channel parameters.** Channel parameters can be set individually for each channel. Programmable parameters include baud rate (50 to 38,400 baud), number of stop bits, parity, and number of data bits per character.
- **User-selectable non-standard baud rates.** Any user-defined baud rate can be substituted for the 1800 baud setting.
- **Level Flow Control.** The CS08/E1 supports hardware assisted level flow control on transmitted data.
- **DMA on transmit.** The CS08/E1 performs word-length DMA transfers on read operations, which halves Q-Bus loading.
- **22-bit addressing.** The CS08/E1 supports the full 22-bit addressing capability of the extended Q-Bus.

Section 2
SUBSYSTEM SPECIFICATIONS

2.1 Overview

This section contains general, physical, and environmental specifications for the CS08/E1 controller module. Specifications for the CP08 Distribution Panels are contained in individual technical manuals. Controller specifications are contained in tables. Including this overview, the section is divided into four main subsections:

Subsection	Title
2.1	Overview
2.2	General and Electrical Specifications
2.3	Physical Specifications
2.4	Environmental Specifications

2.2 General Specifications

Table 2-1 contains general specifications for the CS08/E1 Communications Subsystem.

Table 2-1. CS08/E1 General Specifications

Parameter	Description
Emulation	Provides complete functional emulation of one DEC DHV11 communications multiplexer
Operating System Compatibility	RSX11M, RSX11M+, RSTS/E, Ultrix-11, MicroVMS, Ultrix-32m
Diagnostic Compatibility	DEC CVDHA??, CVDHB??, CVDHC?? for LSI-11
	Emulex IQC09E for MicroVAX I and II
Number of Channels	8
Throughput Rate	60,000 characters per second
Receive Silo	256-character FIFO

(continued on next page)

Table 2-1. CS08/E1 General Specifications (continued)

Parameter	Description
Transmission Modes	Full-duplex, half-duplex
Transmission Speeds	50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200, 38400 bps Non-standard baud rates also supported.
Character Formats	Character lengths: 5 to 8 bit Stop bits: 1, 1.5, or 2 Parity: odd, even, or none
Programmable Split Speed	See Table 7-1.
Modem Signals (CP08/M)	CD, Ring, CTS, DSR, RTS, DTR
Emulex Distribution Panels Supported	CP08/M, CP08/J
Indicators	
CC08 Controller	Fault LED (red)
CP08/M Distribution Panel	Fault LED (red) On-Line LED (green)
CP08/J Distribution Panel	Fault LED (red) On-Line LED (green)
CPU Interface	Standard LSI-11 Bus interface
DMA Address Range	Full 22-bit address range
DMA Transfer	16-bit word with parity check
Device Address	Configurable to all DEC-defined DHV11 device addresses.
Vector Address	Configurable to all DEC defined DHV11 vector addresses.
Priority Level	BR4 or BR5 (configurable)
Electrical	
Power	+5 VDC $\pm$ 5%, 4 amps (typical)
Bus Loading	One LSI-11 Bus load

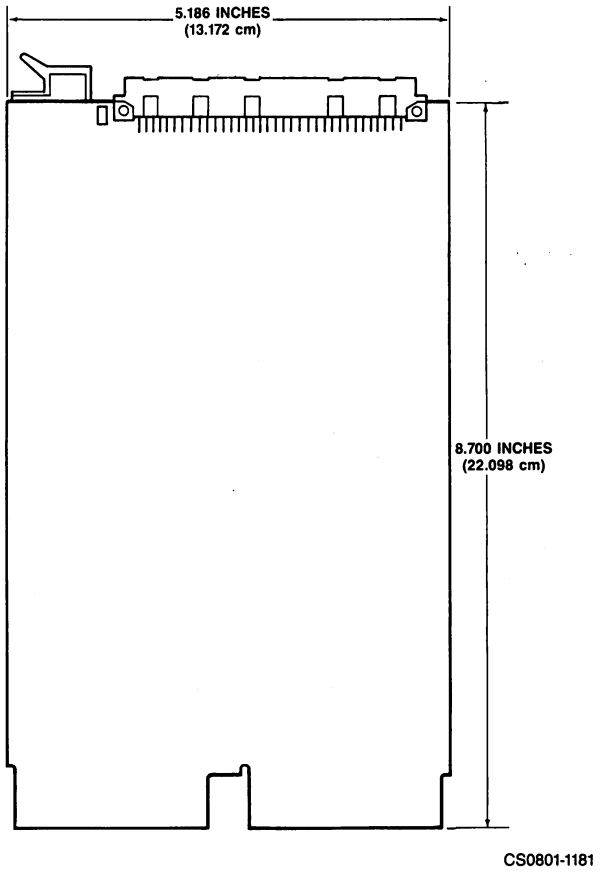


Figure 2-1. CC08 Controller Module Dimensions

2.3 Physical Specifications

Table 2-2 contains physical specifications for the CC08 Controller Module. Figure 2-1 depicts the CC08 Controller Module PCBA.

Table 2-2. CC08 Controller Module Physical Specifications

Parameter	Description
Packaging	Single dual-sized Q-Bus PCBA
Dimensions	5.4 inches x 8.9 inches
Shipping Weight	4 pounds
Connectors	
LSI-11 Bus	Standard DEC PCBA edge connectors
Distribution Panel	One 64-pin header connector

2.4 Environmental Specifications

Table 2-3 contains environmental specifications for the CC08 Controller Module.

Table 2-3. CC08 Controller Module Environmental Specifications

Parameter	Description
Operating Temperature	0°C (32°F) to 45°C (113°F) Maximum temperature is reduced 1.8°C per 1000 meters (1°F per 1000 feet) altitude
Relative Humidity	10% to 95% with a maximum wet bulb of 28°C (82°F) and a minimum dewpoint of 2°C (3.6°F)
Cooling	11 cubic feet per minute
Heat Dissipation	70 BTU per hour

Section 3
INSTALLATION

3.1 Overview

This section describes how to physically install the CS08/E1 Communications Subsystem.

This section **does not** contain every step necessary for bringing up the system. On the next page is an Installation Checklist, which outlines the entire process (covered in detail in this section plus sections 4 and 5). Use this checklist to make sure you complete each step in the installation process.

3.1.1 Maintaining FCC Class A Compliance

Emulex has tested the CS08/E1 Communications Subsystem with DEC computers that comply with FCC Class A limits for radiated and conducted interference (RFI).

The CC08 Controller Module and the CP08 Distribution Panel are designed to be mounted in the same cabinet and thus do not require any special cabling to maintain FCC compliance for radiated interference. It is your reponsibility to make sure that nothing is done that reduces the effectiveness of the cabinet shielding (i.e., there must be no gap in the shield).

Conducted interference is generally prevented by installing a filter in the AC line between the computer and the AC outlet. Most power distribution panels currently manufactured contain suitable filters.

3.2 Inspection

Emulex products are shipped in special containers designed to provide full protection under normal shipping conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the CS08/E1 subsystem and verify that all components listed on the shipping invoice are present (see subsection 1.4 for a list subsystem components and their part numbers). Verify that the model or part number (P/N) designation, revision level, and serial numbers agree with those on the shipping invoice. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

INSTALLATION CHECKLIST

- ☐ 1. Inspect the CC08 Controller and the CP08 Distribution Panel.
- ☐ 2. Install the controller in the backplane of the computer. Follow the instructions for either MicroVAX/MicroPDP-11 computers (section 3.3) or rack-mounted LSI-11 computers (section 3.4).
- ☐ 3. Mount the distribution panel and cable it to the controller. The procedure for doing this is outlined in this manual, but you should refer to the CP08 Technical Manual for more detailed instructions.
- ☐ 4. Run the configuration program. This program, built into the CS08/E1, allows you to choose all subsystem options, such as bus and vector addresses and nonstandard baud rates.
- ☐ 5. Run diagnostics. On an LSI-11 CPU, run the DEC diagnostics. On a MicroVAX CPU, run the Emulex diagnostics.
- ☐ 6. Reconfigure your operating system to include the additional DHV11 emulations.
- ☐ 7. Attach external equipment (terminals, printers, etc.) to the distribution panel. As above, the cabling requirements are outlined in this manual but you should refer to the CP08 Technical Manual for detailed instructions.
- ☐ 8. Bring the system up.

3.2.1 CC08 Controller Module and Distribution Panel Inspection

A visual inspection of the CC08 Controller Module is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. All socketed components should be examined carefully to ensure they are properly seated.

Inspect the distribution panel in the same manner.

3.3 Installation of the CS08/E1 in a MicroVAX or MicroPDP-11

This subsection describes the procedure for mounting and cabling the CS08/E1 in a MicroPDP-11 or MicroVAX. The CS08/E1 subsystem may be mounted in the tabletop, floor-mount or rack-mount DEC MicroPDP-11 or MicroVAX. The following steps describe the installation procedure:

1. Turn off the system power (using the front panel switch) and unplug the AC power cord from the wall.

2. Remove the rear plastic cover of the MicroPDP/VAX to expose the system I/O panel. (The rack-mount version does not have a rear cover.)

3. Using a blade screwdriver, loosen the captive screws that retain the patch panel mounted in the system I/O panel (see Figure 3-1). Lift the panel slightly and pull it out, leaving the cables connected.

   This step is not necessary on a BA123 (World Box) cabinet.

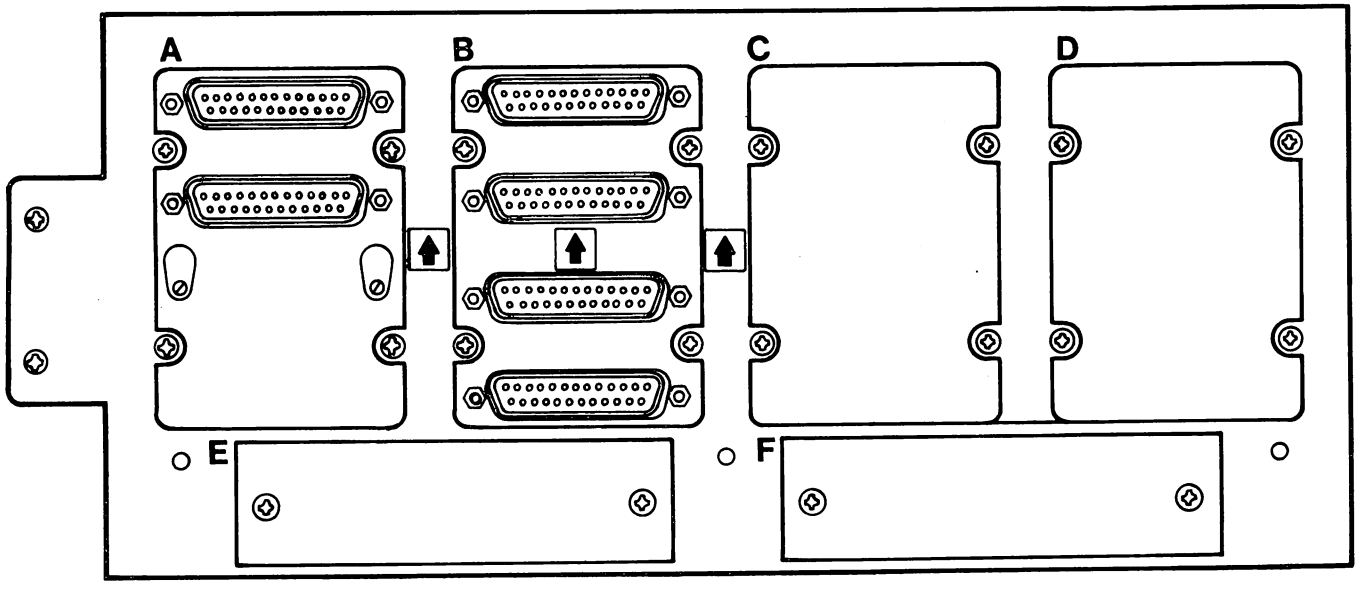


Figure 3-1. MicroPDP-11 or MicroVAX Patch Panel Assembly

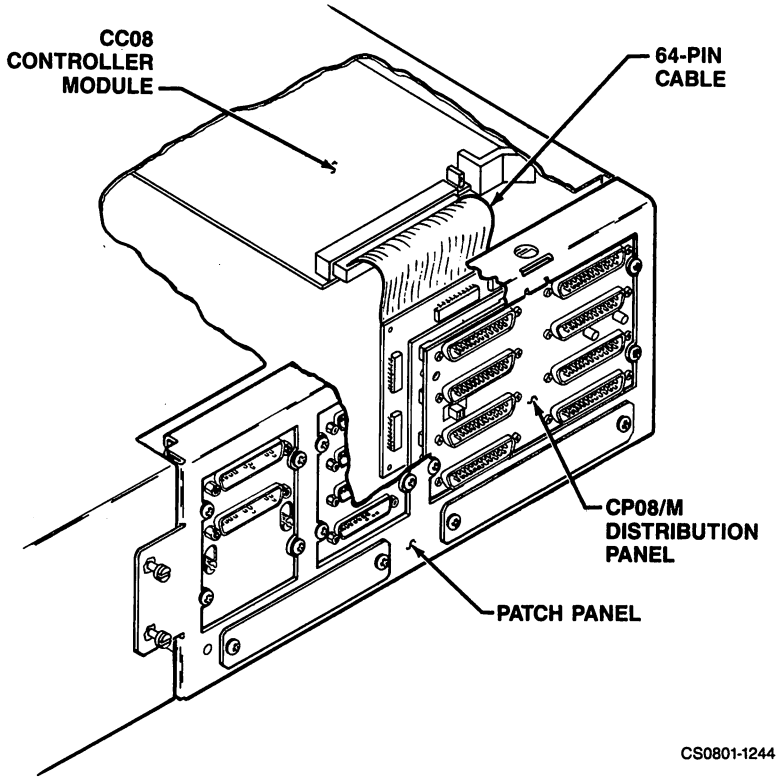


Figure 3-2. Typical Completed MicroVAX Installation (CP08/M)

4. If your system contains an RQDX1 board, it must occupy the last slot in the backplane. Pull it out without removing the cables and move it over one slot.

5. Insert the CC08 Controller Module in the slot from which the RQDX1 was removed, with the components oriented in the same direction as the CPU and other modules in the backplane. The CC08 is a dual wide board and plugs into two backplane connectors; you may insert it into either the top or bottom pair of connectors.

   Depending on the type of backplane your CPU contains, there may be a loss of continuity because of the two empty connectors. If so, plug a grant card (available from DEC) into the connectors beside the CC08.

6. Install and cable the distribution panel. Refer to the appropriate Distribution Panel Technical Manual for instructions on installing and cabling the CP08 in a MicroVAX or MicroPDP-11.

   Figure 3-2 illustrates a typical completed installation of the CS08/E1 subsystem with the CP08/M in a MicroVAX. Figure 3-3 shows the subsystem with the CP08/J.

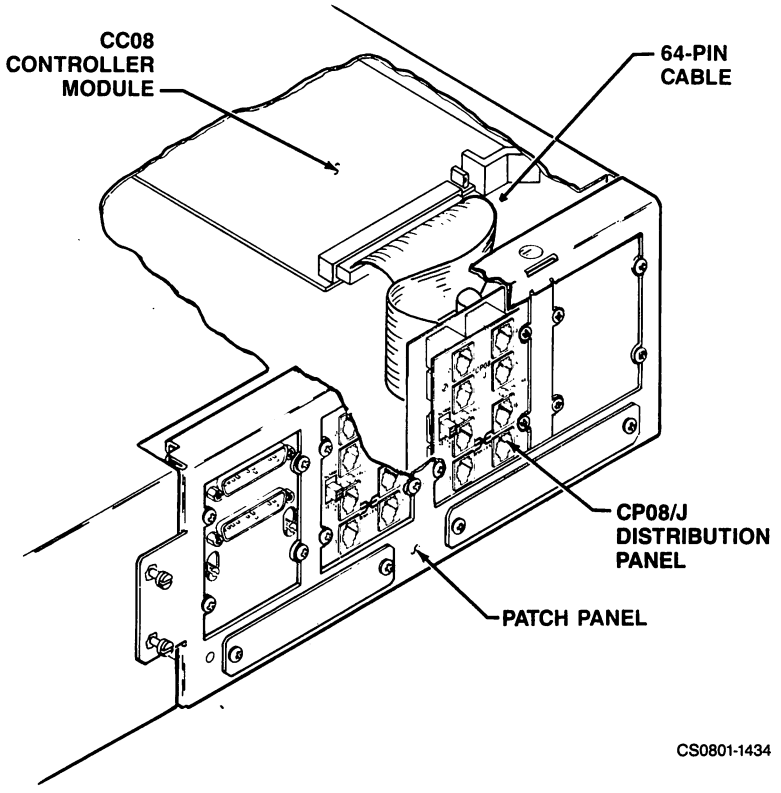


Figure 3-3. Typical Completed MicroVAX Installation (CP08/J)

3.4 Installation of the CS08/E1 in an LSI-11

This subsection describes the procedure for mounting and cabling the CS08/E1 in an LSI-11. The CS08/E1 subsystem may be mounted in either a DEC FCC-compatible CPU or on the RETMA rails of a 19-inch equipment rack. The following steps describe the installation procedure:

1. Turn off the system power and switch OFF the main DC breaker. Remove the side covers from the CPU cabinet and otherwise make the LSI-11 Bus accessible.

2. Install the controller. The CC08 Controller Module can be inserted into either half of any backplane slot in the DEC LSI-11 computer chassis. The closer a module is to the CPU, the higher its interrupt priority.

   As a general rule, the CC08 Controller Module should be placed in front of mass storage peripherals which have large buffers, and behind small disk and tape controllers which have little buffering. There should be no open slots between the CPU module and the last device on the bus.

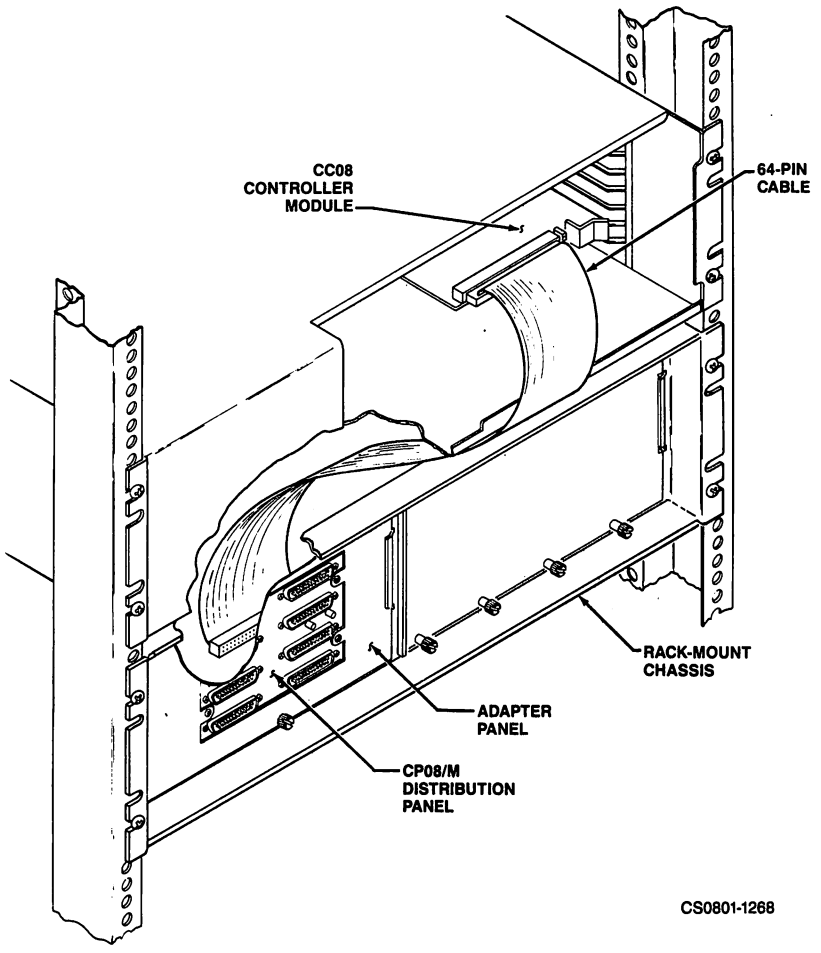


Figure 3-4. Typical Completed LSI-11 Installation (CP08/M)

The controller module must be plugged into the backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the module with the computer power OFF to avoid possible damage to the circuitry. Be sure that the module is properly seated in the throat of the connector before attempting to seat the module by means of the extractor handles.

3. Install and cable the distribution panel. In LSI-11 installations, the CP08 Distribution Panel is designed to mount in one of two places: the rear of a DEC FCC-compatible CPU (in the place of four DEC I/O cutouts) or in an Emulex rack-mount panel (which is mounted on the RETMA rails of a 19-inch equipment rack). See Table 1-2 for Emulex part numbers.

   In both cases, the CP08 must first be mounted in an Emulex rack-mount adapter that allows it to fit in either the DEC I/O cutouts or the rack-mount panel. After it is mounted, the distribution panel is cabled directly to the CC08 Controller via a 64-pin cable.

   Figure 3-4 illustrates a typical installation of the CS08/E1 subsystem with the CP08/M in an LSI-11 system. Figure 3-5 shows the subsystem with the CP08/J. For more detailed installation and cabling instructions, read the installation section of the Distribution Panel Technical Manual.

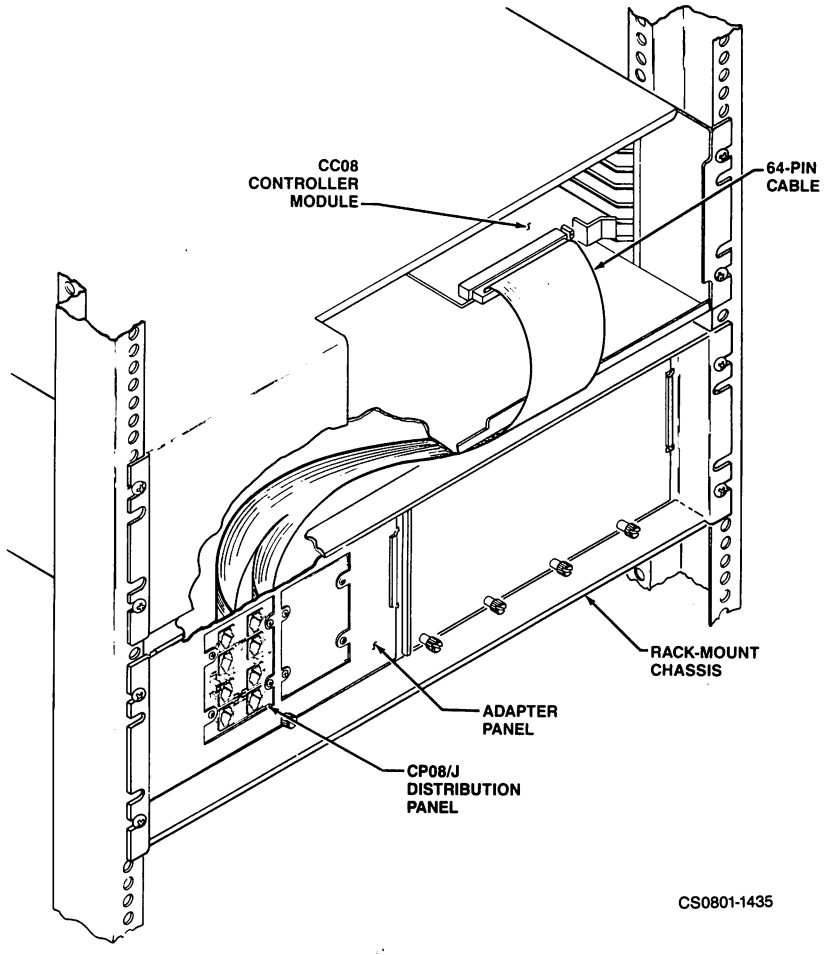


Figure 3-5. Typical Completed LSI-11 Installation (CP08/J)

3.5 Cabling External Devices

The CP08 distribution panels contain RS-232-C serial ports that are used to attach external devices such as modems, printers, and terminals.

Different cabling is required for different applications. Appendix A contains diagrams of terminal cables, modem cables, and null modem cables (used to attach devices directly to the CP08/M and retain full modem control). Refer to the CP08 Distribution Panel Technical Manual for further cabling details.

Section 4
CHOOSING OPTIONS

4.1 Overview

This section describes how to select the subsytem options that are available to the user. These options range from choosing bus and vector addresses to selecting channel parameters such as flow control and nonstandard baud rates.

4.2 Starting the Configuration Process

Unlike most communications controllers, the CS08/E1 has no switches. Instead, all options are chosen via a configuration program built into the CS08/E1 firmware. Once the options are chosen, they are stored permanently in nonvolatile RAM on board the controller.

The configuration program must be run offline, before the system has been brought up. If you wish to change a parameter on a running system, you must first take the system offline. To start the configuration program, follow these steps:

1. Plug a terminal (a CRT is recommended) into any port on the CP08 Distribution Panel. Use the standard terminal cable shown in Appendix A. Any asynchronous terminal will work as long as it meets the following requirements:

   Baud rate = 9600 bps
   Character length = 8 bits
   Parity = none
   Uses no modem control signals
   Does not require level flow control (XON/XOFF flow control is suppported)

2. Place the switch on the front of the CP08 in the SETUP position. The Fault LED starts blinking.

3. Press the <return> key on your terminal. The Main Menu appears on your screen and all other ports on the CP08 become inactive. When you are finished with the configuration, place the CP08 switch back in the NORMAL position. The CS08/E1 is ready for normal operation.

The following sections describe the Main Menu and the Configuration Menu.

On each menu, entries must be followed by <return>. To correct a mistake, use the <delete> key. If you enter a value that is not allowed, the terminal beeps and you are asked to press <return>. You may then enter the value again.

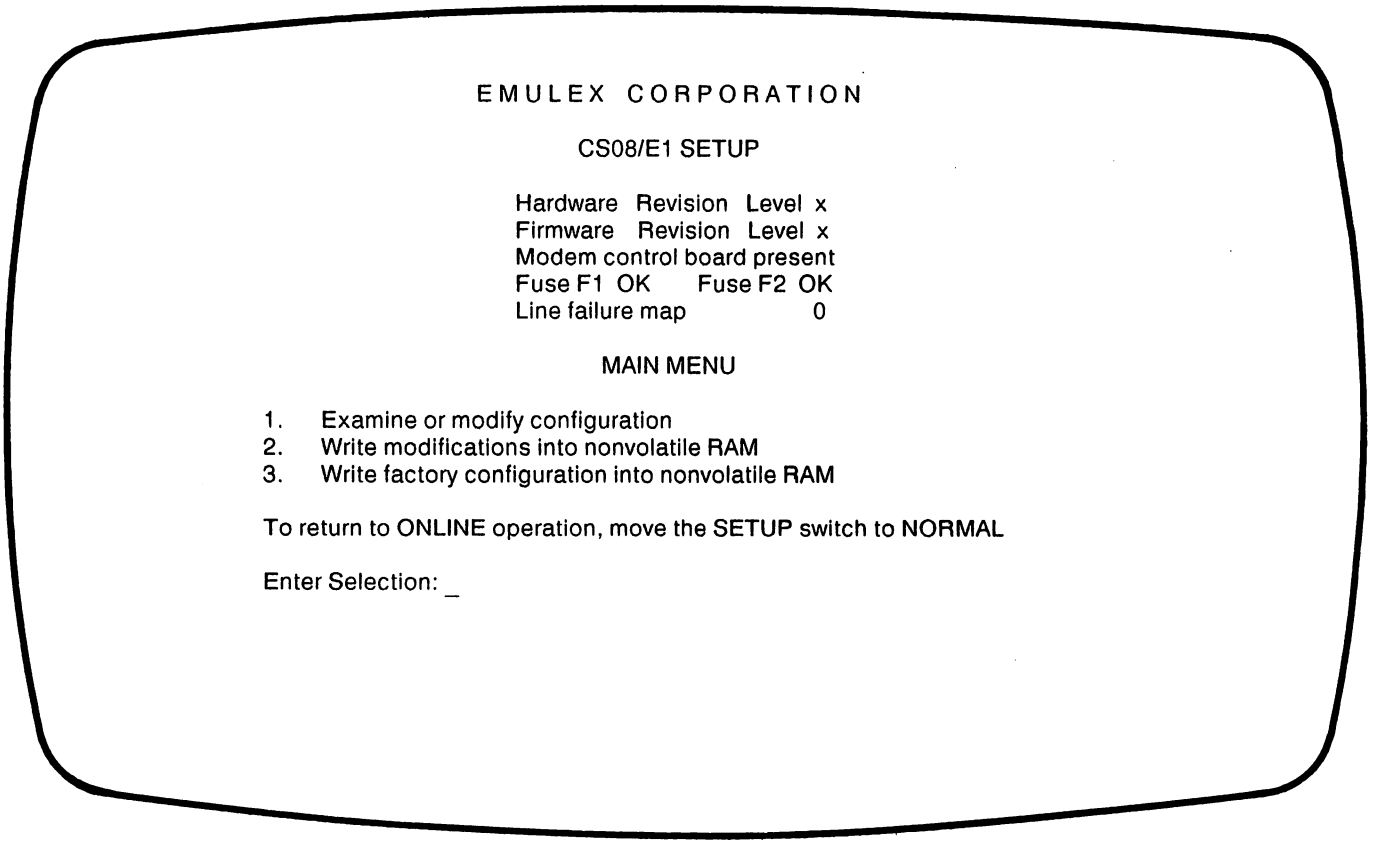


Figure 4-1. Main Menu

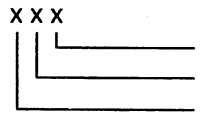
4.3 Main Menu

The Main Menu is shown in Figure 4-1. The top of the menu shows the following things:

- Revision level of the CS08/E1 hardware.
- Revision level of the CS08/E1 firmware.
- The presence of the modem control board, which is attached to the rear of the CP08/M Distribution Panel. If the board is missing (or if you are using the CP08/J), the message does not display.
- The status of two fuses on the controller. These fuses control power to the distribution panel and must both be OK. If either of them is blown, the modem signals on the CP08/M distribution panel will no longer function and the board must be sent in for service.
- A map of nonfunctioning lines. This is displayed as an octal mask that represents the eight lines. If all lines are good, the number displayed is 0. Refer to the box on the next page if you are unfamiliar with octal masks.

CS08/E1 Bad Line Map

The CS08/E1 displays its list of bad lines as an octal line mask. Each digit in an octal line mask corresponds to several lines on the controller, as follows:



Each octal digit corresponds to three binary digits, as follows:

0	= 000	4	= 100
1	= 001	5	= 101
2	= 010	6	= 110
3	= 011	7	= 111

A "1" corresponds to a bad line; a "0" corresponds to a good line. Thus, for example, a line mask of 102 corresponds to:

1	0	2
001	000	010

Counting from right to left, lines 1 and 6 are bad. All others are good.

The Main Menu has three selections. To make a selection, type the number of the selection followed by <return>. The following selections are available:

1. **Examine or modify configuration.** This selection brings up a menu that allows you to choose controller options (such as bus and vector address). It is described in section 4.4.

2. **Write modifications into nonvolatile RAM.** After you have finished the configuration, this selection stores your configuration permanently in the nonvolatile RAM on board the CS08/E1 and prints the message "Nonvolatile RAM has been updated, enter <CR> to continue."

3. **Write factory configuration into nonvolatile RAM.** This selection erases any configuration options previously entered and sets all lines to the factory configuration. The factory configuration is as follows:

   - Starting Address = 160440_8
   - Interrupt Vector = 300_8
   - Number of Emulations = 2
   - Bus Request Level = 4
   - All Emulex options = No

   When the factory configuration is stored, the message "Nonvolatile RAM has been updated, enter <CR> to continue" is printed.

```
                    CS08/E1 CONFIGURATION MENU

<CR> only input = no change

Starting address, modulo 20 (range 160000-177760):                160440
Starting vector, modulo 10 (range 300-770):                       300
Bus request level (4,5):                                         4
Enable Emulex options (Y,N):                                      N
Force two stop bits, global (Y,N):                                N
User defined baud rate, global (range 2-65535, 0 = disable):      0
Break timing, 1 = 1 msec, global (range 1-128, 0 = disable):      0
Level flow control (octal line map, 0 = disable):                 0

Enter <CR> to continue
```

Figure 4-2. Configuration Menu

4.4 Configuration Menu

This menu allows you to select controller options. Each option is displayed one at a time and the current value for the option is listed on the right side of the screen. To select a new value, type the value and press <return>. To leave the current value unchanged, simply type <return>. After you have finished with the last option, press <return> and the Main Menu reappears. You may type <control-c> and <return> at any time to return to the Main Menu.

4.4.1 Starting Address

This option allows you to choose a bus address (in octal) for the CS08/E1. DHV11-type devices are assigned bus addresses from the floating address space of the I/O page. If you are unfamiliar with the rules for assigning bus addresses, see Appendix B for the bus address determination procedure. The allowable range for the bus address is 160000_8 to 177760_8.

4.4.2 Starting Vector

This option allows you to choose an interrupt vector address (in octal) for the CS08/E1. Like the bus address, interrupt vectors for DHV11-type devices are chosen from the floating vector space that starts at 300_8. If you are not familiar with the rules for selecting floating vector addresses, refer to Appendix B.

The allowable range for interrupt vectors is 300_8 to 770_8.

4.4.3 Bus Request Level

This option allows you to choose the bus priority level used by the CS08/E1. The normal BR level for DHV11-type devices is BR4. Level BR5 may be chosen if response time is not adequate due to bus loading problems, but be aware that the priority level of the DHV11 driver must also be changed to match.

4.4.4 Enable Emulex Options

If you answer Y to this menu option, the configuration menu allows you to select the following Emulex options:

- Force two stops bits
- User defined baud rate
- Break timing
- Level flow control

If you answer N, all of these options are disabled. Each option is described in the following subsections.

NOTE

All Emulex options must be off in order to run diagnostics. If you have previously enabled any of them and wish to run diagnostics, step through the menu and answer N to this option. Your old selections will be saved but disabled. When the diagnostics are finished, step through the menu again and answer Y to this option. Your old values will be restored.

4.4.5 Force Two Stop Bits

This option overrides program control of the number of stop bits per character. When this option is selected, all channels will transmit two stop bits with every character. This option is useful in situations where a continuous stream of asynchronous characters is being transmitted and the transmit station's data rate is slightly faster than the receive station's data rate. In these cases one stop bit between characters may not allow enough time for the receiving station to synchronize on the start bit which immediately follows the single stop bit.

The allowable answers are Y (yes) and N (no).

4.4.6 User Defined Baud Rate

This option allows you to choose any baud rate for a channel even if that rate is not supported by the DEC DHV11 or MicroVMS. When this option is selected, any line set for a baud rate of 1800 bps runs at the new rate. This operation is completely transparent to the operating system. When 0 is entered this option is disabled (i.e., lines set for 1800 bps run at 1800 bps).

NOTE

This option is not supported on lines 0 and 1.

The number entered here is **not** the desired baud rate. It is a timer count and the following formula must be used to translate a baud rate into the timer count:

$$\text{Timer count} = \frac{115{,}200}{\text{Baud Rate}}$$

Table 4-1 shows the required timer counts for some common baud rates. Note that MicroVMS may time out if large character blocks are transmitted on channels configured for less than 100 baud.

Table 4-1. Timer Count/Baud Rate Translation

Baud Rate	Timer Count	Baud Rate	Timer Count
50	2304	1800	64
75	1536	2000	58
100	1152	2400	48
110	1047	3600	32
134.5	857	4800	24
150	768	7200	16
200	576	9600	12
300	384	19200	6
600	192	38400	3
1200	96	57600	2

4.4.7 Break Timing

This option allows host software to conveniently time the length of transmitted break signals. It is included for the convenience of system programmers and may be ignored by ordinary users.

Normally, break characters are transmitted from an external device such as a terminal and received by the host computer. In this situation, the external device times the duration of the break sequence.

In certain applications, however, it is necessary for the host computer to transmit a break to an external device or another computer. In this situation, it is the responsibility of the host to control the duration of the break. Because neither the MicroVMS DHV11 driver nor the DHV11 hardware provides a timing funtion for transmitted breaks, timing must be done by a software timer. The drawback to this method is that the timer is dependent on the line's baud rate.

The Emulex break timing option provides a simple method for application programs to time breaks that is independent of the line's baud rate. The program sets the break (BC) bit in the CS08/E1 Line Control Register and transmits a message to control the duration of the break. When the message transmission is complete, the program resets the BC bit, terminating the break sequence.

The formula below defines a time in milliseconds for the transmission of a character (PIO or DMA mode). This transmission time is independent of the line's baud rate:

Break Time (milliseconds) = (Break value) * (number of characters - 1)

For details on programming with this option enabled, refer to the description of the Break Control bit (Line Control Register bit 03) in section 7.2.6.

The break timing option is disabled by entering a 0. If this is done, character transmission is halted during a break (normal DHV11 operation).

4.4.8 Level Flow Control (Transmitted Data Only)

This option is displayed only if a CP08/M distribution panel is present and the modem control board on the rear of the CP08/M is present.

Flow control is used to control the flow of data between the CPU and external devices. XON/XOFF flow control is the method used by DEC and for this reason we recommend using devices that are capable of using XON/XOFF flow control. If all your devices are capable of XON/XOFF flow control, you may disable level flow control by entering the number 0 for this option.

Some devices, however (especially printers), are receive-only devices and are incapable of transmitting XON/XOFF characters. These devices typically use level flow control, in which modem signals are used to start and stop the flow of data.

Level Flow Control Octal Line Mask

Emulex level flow control may be enabled on multiple lines. An octal line mask is used to specify which lines are enabled. To construct the proper mask, translate the line numbers into octal masks:

```
0 = 1
1 = 2
2 = 4
3 = 10
4 = 20
5 = 40
6 = 100
7 = 200
```

Next, add up all the masks. For example, to enable level flow control on lines 0, 3, and 7, add the following masks:

```
  1
 10
200
---
211
```

Thus, 211 is the number to enter at the level flow control prompt on the Configuration Menu.

The DEC DHV11 driver supports level flow control. When it is enabled, the external device lowers its Data Terminal Ready modem signal when it cannot accept more data and raises it when it is once again able to receive data. The DTR pin on the device connects to the CTS pin on the CP08/M Distribution Panel.

The weakness of this approach is that the DHV11 driver cannot always respond quickly enough. Some devices (for example, some terminals, plotters, and printers) require that transmission be halted very quickly. For these devices, you must enable Emulex level flow control.

The Emulex level flow control option assists the standard DHV11 flow control by sensing the modem signals and stopping transmission when CTS is negated. The CS08/E1 will always stop transmission within two characters.

Level flow control is selected on a per-line basis by entering an octal mask. To disable level flow control completely, enter the number 0. If you are unfamiliar with octal masks, refer to the box at the top of this page.

There are several things you should be aware of if you enable this option under MicroVMS:

1. Lines using level flow control must be set up for modem operation.

2. A special cable must be used between the CP08/M and the external device that loops back certain modem signals and prevents MicroVMS from timing out. Refer to Appendix A for a schematic of the necessary cable. Note that a 25-pin connector is shown on the terminal end of the cable.

Section 5
OPERATION

5.1 Overview

This section describes two things:

- **Diagnostic operation.** Before you bring the system online, you should run either DEC or Emulex diagnostics to insure that the CS08/E1 is functioning properly.

- **Operating system configuraton.** Your operating system must be reconfigured to include the new DHV11 emulations. Once this step is finished, you may bring up the system and begin normal operation.

5.2 Diagnostics

Emulex supplies diagnostics that test each component of the CS08/E1 subsystem, including all aspects of controller operation, distribution panel operation, and line integrity. Two types of diagnostics are available:

- For LSI-11 CPUs, Emulex distributes standard DEC DHV11 diagnostics (CVDHA??, CVDHB??, and CVDHC??). For instructions on running these diagnostics and installing the patches, refer to Appendix C.

- For MicroVAX CPUs, Emulex supples a diagnostic (IQC09E) that runs under MicroEVM, the Emulex MicroVAX Monitor. Instructions for running both the monitor and the diagnostic are included with the diagnostic media.

All of these diagnostics are offline utilities, so be sure to run them before you bring the system up.

5.3 Operating Systems

Before you can bring up the system, you must reconfigure your operating system to include the new DHV11 emulations. Although this manual cannot include complete instructions for generating DEC operating systems, the following sections contain outlines of the procedure under RSTS/E, RSX-11M, RSX-11M-PLUS, Ultrix-11, MicroVMS, and Ultrix-32m. Read only the section that applies to your operating system.

NOTE

If the CS08/E1 is installed in a system running under MicroVMS, be sure you have a license for as many channels as you are planning to use. MicroVMS can be licensed for as few as two users or as many as 32 or more.

5.3.1 Bus and Vector Addresses

All operating systems, as part of the SYSGEN procedure, ask you for the bus and vector addresses of the device you are adding. You must respond with the addresses that are programmed into the CS08/E1 via the configuration program (see section 4). Your response depends on the operating system you are using:

- Under RSTS/E, RSX-11M, RSX-11M-Plus, and Ultrix-11, you can generally assign any address that does not conflict with other devices in your system. If you use autoconfigure, you must choose addresses that conform to what autoconfigure expects. Appendix B explains the autoconfigure algorithm.

- Under MicroVMS, autoconfigure is almost always used. In order to make this more convenient, MicroVMS contains a utility that calculates bus and vector addresses automatically. Appendix B explains how to use this utility and also explains how to calculate the addresses manually if you do not have access to a running MicroVMS system.

- Under Ultrix-32m, you assign only the bus address. SYSGEN then forces an interrupt to discover what interrupt vector is programmed into the board. You must make sure that neither the bus or vector addresses conflict with other devices in the system.

5.3.2 Adding a New Device to RSTS/E

All device drivers are an integral part of the RSTS/E monitor. Therefore, when you add a new device to your system, you must generate an entirely new RSTS/E monitor. You do not need to generate a new monitor if either of the following two conditions is true:

- You are merely replacing an existing device with an Emulex emulation of the same device. That is, if you already have a DEC DHV11 and you are replacing it with a CS08/E1, there is no need to regenerate the RSTS/E monitor.

- Your present RSTS/E monitor already includes support for DHV11s but it has been disabled. To enable it, simply type HARDWARE at the INIT.SYS option prompt and answer ENABLE at the HARDWARE suboption prompt. When it asks "Controller to Enable," answer VH0 (the RSTS/E mnemonic for DHV11). To end, type Exit.

5.3.2.1 Generating a New Monitor With SYSGEN

If your RSTS/E monitor does not include support for DHV11s, you must generate a new RSTS/E monitor that includes DHV11 support. To do this, you must generate a new monitor as described in the DEC *RSTS/E System Generation Manual*. If the only change you are making to your system is to add the CS08/E1, then most of your answers to the SYSGEN questions will not change. The only changes will be made during the Terminal Interface Configuration stage. The questions relating to the CS08/E1 are the following:

- DHU11/DHV11's? <x>
  Answer: 1.

- DHU11/DHV11 unit 00 lines enabled? <8>
  Answer: 8.

- Dataset support for DHU11/DHV11's? <N>
  Answer: Yes, if you require auto-answer modem support.

Complete the monitor building as described in the DEC *RSTS/E System Generation Manual*.

5.3.2.2 Assigning Bus and Vector Addresses

If you have followed the standard autoconfigure procedure for assigning bus and vector addresses, RSTS/E will find all the devices in your system and power up correctly. However, if you have assigned nonstandard addresses, you must use the HARDWARE CSR and HARDWARE VECTOR commands to tell RSTS/E where the devices reside. Use the following procedure to reassign the bus address for a device:

- At the INIT.SYS Option prompt, type HARDWARE.
- At the HARDWARE suboption prompt, type CSR.
- RSTS/E asks, "Controller with non-standard address?" Respond with the mnemonic of the controller. For the CS08/E1, the mnemonic is VH0.
- RSTS/E asks, "New controller address?" Respond with the address you have assigned.
- Press <control-z> to return to the HARDWARE suboption prompt.

Once the bus address has been specified, RSTS/E pokes the device to discover what interrupt vector is being used. You can set the interrupt vector manually by following the procedure above and typing VECTOR at the HARDWARE suboption prompt instead of CSR.

5.3.2.3 Modem Controls

After the RSTS/E monitor is complete, you must configure each CS08/E1 line as either local or remote. To enable modem controls for one or more lines:

RSTS/E versions 9.0 and above

During SYSGEN, enable dataset support. Then, for each line requiring modem support, enter the following line in the startup command file:

```
SET TERM/PERM/DIALUP KBx:
```

RSTS/E version below 9.0

- At the INIT.SYS Option prompt, type SET.
- At the SET suboption prompt, type LIST.
- At the Device prompt, type KB. The computer's response will be a list of all DHV11 lines and the keyboard numbers associated with each line. Note down the keyboard numbers of all lines that will require modem support. Lines are numbered from 0, starting with the controller at the lowest bus address. The lines associated with the CS08/E1 are numbered starting with port 0 on the CP08 and going up to port 7.
- At the SET suboption prompt, type MODEM.
- At the KB prompt, type the keyboard numbers you noted down above. If you frequently switch modems from line to line, you may enable modem controls for all lines by typing a range. For example, if the DHV11 emulation of the CS08/E1 were assigned keyboard numbers 8 through 15,

then typing 8-15 at the KB prompt will enable modem controls on all lines. If you do this, be sure to follow the null-modem cabling instructions in the distribution panel technical manual.

- Bring up the system. At the $ prompt, type

  SET KB??:/DIALUP

  This should be added to the system startup file so that this characteristic is set each time the system is booted.

5.3.3 Adding a New Device to RSX-11M

In general, when a new device is added to the RSX-11M operating system, a completely new operating system must be generated. You do not need to do this if you already have a DEC DHV11 installed and are merely replacing it with a CS08/E1.

If you are making no other changes to your system, then most of your answers to the SYSGEN questions will remain the same. The SYSGEN Phase I questions that relate to the CS08/E1 are the following:

- Autoconfigure the host system?
  Answer: Yes, if you wish to use autoconfigure.

- Devices.
  Answer: SYSGEN will print a list of the devices it found during the autoconfigure process. If it is correct, simply type a period. The RSX-11M mnemonic for a DHV11 is YV, so autoconfigure should include YVA if the CS08/E1 is the only DHV11 in your system.

- Loadable device drivers?
  Answer: Yes. The DHV11 requires a loadable driver.

- Terminal driver desired.
  Answer: Full-duplex

- YV controller 0.
  Answer: This question asks for the vector address, bus address, number of lines, and the default baud rate for remote lines. Autoconfigure should provide the correct responses already, which will look something like this:

  300,760020,8,300

  If the listed values are not correct, enter the correct values. Note that the default baud rate can be changed after SYSGEN is completed if you wish. If you do not want modem support, enter a default baud rate of zero.

After you have finished the Phase I questions, you must complete Phases II and III as described in the DEC *RSX-11M System Generation Manual*.

5.3.3.1 Modem Controls

The MCR command SET can be used to change a terminal's status from remote to local and vice versa. It can also be used to change the baud rate of an individual channel. The command

```
SET /REMOTE
```

lists all remote channels. The command

```
SET /REMOTE=TT5:1200
```

sets the terminal line corresponding to TT5 as a remote dial-up line with a baud rate of 1200. To configure a line for autobaud operation, set the line for 0 baud and then set it for autobaud operation:

```
SET /REMOTE=TT5
SET /ABAUD=TT5
```

Configuring lines for local operation works the same way. The command

```
SET /NOREMOTE
```

lists all local channels, and the command

```
SET /NOREMOTE=TT5:
```

sets the terminal line corresponding to TT5 as a local line. To find out which DHV11 line corresponds to TTn, you must check your hardware to see which terminals are connected to which ports on the distribution panels. Any user may use the SET command to change his own line, but only a privileged user may change another channel's characteristic.

Some users enable modem controls for all channels because they are constantly switching modems from channel to channel. If you do this, be sure to follow the null-modem cabling instructions in the distribution panel technical manual.

5.3.4 Adding a New Device to RSX-11M-Plus

To add a new device to the RSX-11M-Plus operating system, the appropriate device driver must be added to the RSX-11M-Plus kernel. Most devices can be added to RSX-11M-Plus without doing a new SYSGEN. However, this is not the case with communications equipment. When you add the CS08/E1, you need to generate a completely new operating system.

If you are making no other changes to your system, most of your answers to the SYSGEN questions will remain the same. The SYSGEN questions which relate to the CS08/E1 are the following:

- Enter number of DHU11/DHV11 asynchronous line multiplexers.
  Answer: 1.

- Enter total number of DHU11/DHV11 dial-up lines.
  Answer: List the number of lines that require modem support. These lines will be the first lines on your system (i.e., the lowest numbered channels). If you specify zero, modem support is excluded.

- Enter total number of DHU11/DHV11 local lines.
  Answer: All lines are either local or dial-up. So, if you specified any dial-up lines, specify the rest as local lines. For example, if you specified 6 dial-up lines, channels DHV0,0 through DHV0,5 would be dial-up lines and channels DHV0,6 through DHV0,7 would be local lines. Lines are numbered from 0, starting with the controller at the lowest bus address. The lines associated with the CS08/E1 are numbered starting with port 0 on the CP08 and going up to port 7.

- Enter vector address of YVA.
  Answer: this is the interrupt vector address programmed into the CS08/E1. YV is the RSX-11M-Plus mnemonic for DHV11.

- What is its CSR address?
  Answer: this is the bus address programmed into the CS08/E1.

- Enter terminal type for YVA.
  Answer: respond with the terminal types you are using. This can be changed later without doing a new SYSGEN, so choose the default answer if you are not sure what terminal types you will be using.

5.3.4.1 Modem Controls

The MCR command SET can be used to change a terminal's status from remote to local and vice versa. It can also be used to change the baud rate of an individual channel. The command

```
SET /REMOTE
```

lists all remote channels. The command

```
SET /REMOTE=TT5:1200
```

sets the terminal line corresponding to TT5 as a remote dial-up line with a baud rate of 1200. To configure a line for autobaud operation, set the line for 0 baud and then set it for autobaud operation:

```
SET /REMOTE=TT5
SET /ABAUD=TT5
```

Configuring lines for local operation works the same way. The command

```
SET /NOREMOTE
```

lists all local channels, and the command

```
SET /NOREMOTE=TT5:
```

sets the terminal line corresponding to TT5 as a local line. To find out which DHV11 line corresponds to TTn, you must check your hardware to see which terminals are connected to which ports on the distribution panels. Lines are numbered from 0, starting with the controller at the lowest bus address. The lines associated with the CS08/E1 are numbered starting with port 0 on the CP08 and going up to port 7. Any user may use the SET command to change his own line, but only a privileged user may change another channel's characteristic.

Some users enable modem controls for all channels because they are constantly switching modems from channel to channel. If you do this, be sure to follow the null-modem cabling instructions in your distribution panel technical manual.

5.3.5 Adding a New Device to Ultrix-11

To add support for DHV11s to Ultrix-11, you must generate a new monitor. The SYSGEN questions that relate to the CS08/E1 are the following:

- Communications devices:
  <dz dzv dzq dh dhu dhv dhdm du dn kl dl>?
  Answer: dhv

- Number of units?
  Answer: 1.

- CSR address for unit 1 <xxxxxx>?
  Answer: this is the bus address programmed into the CS08/E1. Press return if the default address provided by autoconfigure is correct.

- Vector address for unit 1 <xxxxxx>?
  Answer: this is the vector address programmed into the CS08/E1. Press return if the default address provided by autoconfigure is correct.

For more details on the SYSGEN process, refer to the *Ultrix-11 System Installation Guide*.

5.3.5.1 Enabling Terminals and Modem Controls

Ultrix-11 uses three types of files to specify the number of lines and the characteristics of each line.

The first file type must be created on a per-line basis. These files are created via the msf command in the /dev account. For example, the following command creates eight files, one for each line of the DHV11 emulation:

```
# msf  dhv11  1  tty00
```

The files created are named /dev/ttyxx where xx is the terminal number.

The second file type is the /etc/ttys file. This file must be edited to specify which lines are active and what speed they default to. The format of each entry in the file is ncttyxx, where xx is the line number, n specifies the type of line, and c specifies the default line speed. The following example shows a typical /etc/ttys file:

```
22console
22tty00
22tty01
22tty02
22tty03
22tty04
22tty05
22tty06
22tty07
```

The third file type is the /etc/ttytype file. This file must be edited to intitialize TERM variables at login time. You must include an entry in this file for each line that is enabled for logins. The following example shows a typical /etc/ttytype file:

```
vt100 console
vt100 tty00
vt100 tty01
vt100 tty02
vt100 tty03
vt100 tty04
vt100 tty05
vt100 tty06
vt100 tty07
```

For further details on configuring these files, refer to the *Ultrix-11 System Management Guide*.

5.3.6 Adding a New Device to MicroVMS

The CS08/E1 is automatically supported by MicroVMS if its bus address and interrupt vector are set for the values required by autoconfigure. The only further requirement is that a command to initiate autoconfigure during power-up must be included in one of several start up command files on the system. As shipped by DEC, this command is located in the STARTUP.COM file located in the SYS$SYSTEM directory. The command syntax is as follows:

```
$RUN SYS$SYSTEM:SYSGEN
AUTOCONFIGURE ALL
```

It is a good idea to set the default line parameters for each channel at the time that it is connected, as shown in Figure 5-1. Set the default parameters for remote channels just as you would for local channels. If a modem is to be connected to either a local or remote channel, set the MODEM and HANGUP switches as shown for TXA0:.

```
$!  TXA0: IS CONNECTED TO A DIAL UP LINE AND A MODEM
$!
$SET TERMINAL TXA0:/SPEED=1200/MODEM/HANGUP/VT100/PERM
$!
$SET TERMINAL TXA1:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA2:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA2:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA3:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA4:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA5:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA6:/SPEED=9600/PERM/VT100
$SET TERMINAL TXA7:/SPEED=9600/PERM/VT100
```

Figure 5-1. DHV11 Line Parameter Default File

5.3.6.1 Modem Controls

Modem controls can be enabled on individual lines via the SET TERM command. For example, to set a line for remote operation use the MODEM qualifer:

```
SET TERM/MODEM
```

To set the baud rate, use the SPEED qualifier:

```
SET TERM/SPEED=1200
```

To set a terminal for autobaud operation, use the AUTOBAUD qualifer:

```
SET TERM/AUTOBAUD
```

If a line is configured for modem operation and you wish to change it to a local line, use the NOMODEM qualifier:

```
SET TERM/NOMODEM
```

NOTE

For all these commands, you must also use the PERM qualifer if you want to permanently change the line configuration.

5.3.7 Adding a New Device to Ultrix-32m

Ultrix-32m supports a maximum of 16 DHV11 lines (two DHV11s). These DHV11s must be included in a configuration file that is used by the Ultrix-32m monitor at SYSGEN time. For example, the configuration file entry for two DHV11s would look something like this:

```
device dhu0 at uba0 csr 0160440 flags 0xff vector dhurint dhuxint
device dhu1 at uba0 csr 0160460 flags 0xff vector dhurint dhuxint
```

The device name "dhu" is used for compatibility with larger VAX CPUs. The flags are binary encoded values that specify which terminals are hard-wired.

At autoconfigure time, Ultrix-32m searches for each device included in the configuration file. When a device is found, a message such as the following is printed:

```
dhu0 at csr 160440 vec 300, ipl 17
dhu1 at csr 160460 vec 310, ipl 17
```

For more information on configuring an Ultrix-32m monitor, refer to the *Ultrix-32m System Manager's Guide*.

5.3.7.1 Enabling Terminals and Modem Controls

Ultrix-32m uses three types of files to specify the number of lines and the characteristics of each line.

The first file type must be created on a per-line basis. These files are created via the MAKEDEV command in the /dev account. For example, the following command creates eight files, one for each line of the CS08/E1:

```
# makedev dhv0
```

The files created are named /dev/ttyhx, where x is the terminal number.

The second file type is the /etc/ttys file. This file must be edited to specify which lines are active and what speed they default to. The format of each entry in the file is ncttyhx, where x is the line number, n is the terminal status (1 = line enabled for logins, 0 = line not enabled for logins), and c determines the default line speed. The following example shows a typical /etc/ttys file:

```
12console
12ttyh0
12ttyh1
12ttyh2
12ttyh3
12ttyh4
12ttyh5
12ttyh6
12ttyh7
```

The third file type is the /etc/ttytype file. This file must be edited to intitialize TERM variables at login time. You must include an entry in this file for each line that is enabled for logins. The following example shows a typical /etc/ttytype file:

```
vt100 console
vt100 ttyh0
vt100 ttyh1
vt100 ttyh2
vt100 ttyh3
vt100 ttyh4
vt100 ttyh5
vt100 ttyh6
vt100 ttyh7
```

For further details on configuring these files, refer to the *Ultrix-32m System Manager's Guide*.

6.1 Overview

This section describes how to isolate problems with the CS08/E1 by using the diagnostic self-test built into the controller.

6.1.1 Service

The components of your Emulex CS08/E1 Communications Subsystem have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory.

Should one of these fault isolation procedures indicate that a component is not working properly, the component must be returned to the factory or one of Emulex's authorized repair centers for service. Emulex products are not designed to be repaired in the field.

Before returning the component to Emulex, whether the product is under warranty or not, you must contact the factory or the factory's representative for instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN A COMPONENT TO EMULEX WITHOUT AUTHORIZATION. A component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii contact:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714)662-5600 TWX 910-595-2521

Outside of the United States, contact the distributer from whom the subsystem was initially purchased.

To help you efficiently, Emulex or its representative requires certain information about our product and the environment in which it is installed. Before you call, be sure to have ready the parameters you have chosen for the CS08/E1 as well as the type of CPU it is installed in.

After you have contacted Emulex and received an RMA, package the component (preferably using the original packing material) and send the the component **POSTAGE PAID** to the address given you by the Emulex representative. The sender must also insure the package.

6.1.2 Test Connector

Some software diagnostics require wrap-around connectors or staggered loopback cables for the distribution panel. You may build these yourself or order them from Emulex. Schematics for the proper wrap-arounds and staggered loopbacks are contained in Appendix A.

6.2 Fault Isolation Procedures

When the CS08/E1 is powered up it turns on the red Fault LED on the CP08 Distribution Panel and executes a self-test that checks the controller circuitry and the distribution panel. After the self-test finshes, the two CP08 LEDs can have the following states:

- Red Fault LED OFF, green Online LED ON: Normal operation. The self-test has passed successfully.
- Both LEDs OFF: Check to make sure CPU power is on, the CC08 is seated correctly in the backplane, and the cable between the CC08 and the CP08 is good. If these all check out positive, the CC08 is probably bad.
- Fault LED ON, Online LED OFF: The CP08 switch is probably in the RESET position. If the Fault LED remains on when the switch is in the NORMAL position, the CC08 is probably bad.
- Fault LED flashing: The switch on the front of the distribution panel is in the SETUP position. Move it to the NORMAL position.

If the self-test detects no failures, the green Online LED lights and everything should work normally. If the LEDs are normal, but there is still a problem with the subsystem (for example, terminals not responding), check the following things:

1. Make sure CPU power is ON.
2. Use the CS08/E1's internal configuration program to test the controller. First, set up a terminal as described in section 4.2. Then plug the terminal into one of the ports, place the CP08 switch in the SETUP position, and press <return>. The Main Menu of the configuration program should come up.

   If the Main Menu does not appear, plug the terminal into another port, toggle the CP08 switch to RESET and back to SETUP, press <return>, and see if the Main Menu appears. If it does, the port that did not respond is bad, so check the line failure map to see if it shows a bad line. If a bad line is shown, the CC08 is bad; if no bad line is shown, either the cable or the CP08 connector may be bad.

3. Check the Main Menu to see if either of the CC08 fuses are bad. If either of them is bad, it means that the power leads from the CC08 to the CP08 have been shorted. The most likely cause is a bad CP08 Distribution Panel, so you must return both the CC08 and the CP08 to Emulex for repair.

   Before you reinstall the CC08 after it has been repaired, be sure to correct the problem that caused the short circuit. The likely causes are bent pins on the CC08 or CP08 connectors, causing one pin to touch another, or a shorted cable between the CC08 and CP08.

4. If the Main Menu does not appear on any of the ports, the problem probably lies in one of the following areas:

   - **The terminal cable.** Standard terminal cables require that the transmit and receive lines be crossed. Terminals that use modem controls require a null-modem cable if they are connected directly to the distribution panel. The schematics in Appendix A show the correct wiring for both types of cables.

     If the cable is the correct type, it still may be shorted or otherwise faulty. Exchange cables and see if this solves the problem.

   - **The terminal.** Make sure it is set up with the parameters listed in section 4.2. If it is, try exchanging it for another terminal and see if that solves the problem.

     During normal operation, the terminal must be set with the same parameters as your terminal driver software. Refer to your terminal's technical manual for information on setting baud rates and for other troubleshooting procedures.

   - **The CP08 cable.** Check the cable between the CC08 Controller and the CP08 Distribution Panel. Test the cable with a multimeter or simply exchange the suspect cable with another and see if that solves the problem.

5. If all of the above tests check out but the system is still not responding, the problem may be that the bus address or interrupt vector address has not been set correctly. Appendix B explains how to select these addresses correctly and section 4 explains how to program the addresses into the CS08/E1 via the configuration program.

If none of these procedures isolates the problem, run the software diagnostics. They are able to discover problems that may not show up on the self-test. If this also does not isolate the problem, call Emulex Technical Support at the address and phone number given at the beginning of this section.

6.3 Power-Up Self-Test

6.3.1 CC08 Controller Module Self-Test

The power-up self-test is a thorough check of the CC08's functional integrity. Three functional areas are checked:

1. The on-board RAM memory
2. The DUARTs
3. The microprocessor itself

When power is applied to the CPU the controller automatically executes its self-test. The test is not executed with every bus INIT but only on power-up (i.e., DCLO asserted).

During the self-test the Fault LED on the front of the CP08/M Distribution Panel is ON. If the self-test is completed successfully, the on-board microprocessor turns the Fault LED OFF. If the LED goes ON when power is applied and stays ON, the CC08 has failed its self test.

When the Fault LED is on, the controller cannot be addressed by the CPU.

Section 7
DEVICE REGISTERS AND PROGRAMMING

7.1 Overview

This section contains a detailed description of the device registers which are accessible to the LSI-11 Bus that are used to monitor and control the CS08/E1 Communications Subsystem. The registers are functionally compatible with those of a DEC DHV11 communications multiplexer.

This section also includes some general programming notes designed to aid the programmer who writes software to operate the CS08/E1, and a brief architectural description of the CC08 Controller Module. The subsections include:

Subsection	Title
7.2	DHV11 Registers
7.3	DHV11 General Programming Notes
7.4	Architecture

For quick reference, Figure 7-1 illustrates the entire DHV11 register set. The bit mnemonics are the same as those used in the more complete descriptions that follow.

The register address is given in terms of an offset from the device's base address. Simply add the offset to the base address to obtain the correct address for a specific register (base addresses and offsets are in octal notation).

7.2 DHV11 Registers

The DHV11 registers occupy eight words in the floating address section of the Q-Bus I/O page. The first two registers are used by all eight lines of the DHV11. The other six registers are replicated eight times, once for each line. The index parameter for these registers is the Indirect Address Register Pointer (Ind. Add. Reg.), (bits <02:00>) in the CSR.

CONTROL STATUS REGISTER (CSR) +0 Octal

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R TA	R/W TIE	R DF	R TDE	0	Tx Line No. R			R RDA	R/W RIE	R/W MR	1	0	Ind.Add. Reg. Ptr. R/W		

RECEIVER BUFFER (RBUF) +2 Octal

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R DV	R OE	R FE	R PER	0	Rx Line No. R			Received Character R							

TRANSMIT CHARACTER BUFFER (TXCHAR) +2 Octal (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W TDV	0	0	0	0	0	0	0	Transmit Character W							

LINE PARAMETER REGISTER (LPR) +4 Octal(Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Tx Data Rate R/W				Rx Data Rate R/W				R/W SC	R/W EP	R/W PE	Char. Length R/W		Diag. Code R/W		0

LINE STATUS (STAT) +6 Octal (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R DSR	0	R RI	R DCD	R CTS	0	0	0	0	0	0	0	0	0	0	0

LINE CONTROL (LNCTRL) +10 Octal (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	R/W RTS	0	0	R/W DTR	R/W LT	Main. Mode R/W		R/W FXO	R/W OAF	R/W BC	R/W RE	R/W IAF	R/W TDA

TRANSMIT BUFFER ADDRESS 1 (TBUFFAD1) +12 Octal (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Buffer Address - Least Significant Part R/W															

TRANSMIT BUFFER ADDRESS 2 (TBUFFAD2) +14 Octal (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W TE	0	0	0	0	0	0	0	R/W TDS	0	Tx Buffer Address R/W					

TRANSMIT DMA BUFFER COUNTER (TBUFFCT) +16 Octal (Indexed by Ind.Add.Reg.)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DMA Character Count R/W															

CS0801-0149

Figure 7-1. DHV11 Registers

7.2.1 Control Status Register (CSR) +0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TA	TIE	DF	TDE	0	Tx Line No.			RDA	RIE	MR	1	0	Ind. Add. Reg. Ptr.		

Read/Write, Byte Addressable

Transmitter Action (TA) - Bit 15

Read-Once

Cleared by Master Clear or by reading the CSR

This bit is set by the controller when:

- the last character of a DMA buffer has left the DUART.
- a DMA transfer has been aborted by the program.
- a DMA transfer has been terminated because of a non-existent memory being addressed or because of a memory parity error.
- a single-character programmed output has been accepted (i.e., the character has been taken from the transmit buffer).

NOTE

CSR contents should not be changed by read-modify-write instructions, such as BIS, BIC, INC, or DEC. These instructions may lose the state of the TA bit.

Transmit Interrupt Enable (TIE) - Bit 14

Read/Write

When set, this bit allows interrupts to occur at the transmit interrupt vector when TA (bit 15) becomes set.

Diagnostics Failure (DF) - Bit 13

Read-Only

When set, this bit indicates that the internal diagnostics have detected an error. The error may have been detected by the self-diagnostic or by BMP (see section 7.3.7). When this bit is set, the Fault LED on the CC08 is turned ON; when it is cleared, the Fault LED is turned OFF.

This bit is set by Master Reset and cleared only after the internal diagnostics have been completed successfully.

This bit is valid only after the Master Reset (bit 05) has been cleared.

Transmit DMA Error (TDE) - Bit 12

Read-Only

When TA (bit 15) is set, setting of this bit indicates that the channel designated by Tx Line Number (bits <11:08>) has failed to transfer DMA data within 12.0 microseconds of the bus request being acknowledged, or that there is a memory parity error. TBUFFAD1 and TBUFFAD2 registers will contain the address of the memory location which could not be accessed. TBUFFCT will be cleared.

Transmit Line Number - Bits <10:08>

Read-Once

If TA (bit 15) is set then these bits contain the number of the line which has just:

- completed a DMA block transfer
- accepted a single character for transmission
- aborted a DMA block transfer.

If TDE (bit 12) is also set, these bits contain the binary number of the channel which has failed during a DMA transfer.

Receive Data Available (RDA) - Bit 07

Read-Only

When set, this bit indicates that a received character is available. This bit is clear when the FIFO buffer is empty. It is used to request an receive interrupt.

This bit is set after Master Reset because the FIFO buffer contains diagnostic information.

Receive Interrupt Enable (RIE) - Bit 06

Read/Write

When set, this bit allows the controller to interrupt the CPU at the receive interrupt vector when RDA (bit 07) has been set. An interrupt is generated if this bit is set and a character is placed in an empty FIFO buffer, or if the FIFO buffer is not empty and this bit is changed from zero to one.

This bit is cleared by BINIT, but not by Master Reset.

Master Reset (MR) - Bit 05

Read/Write

This bit is used to reset the emulation to a known state. After being set by the CPU, this bit will remain set while the controller is performing the reset function; it is cleared to zero when the reset function is complete. A Master Reset initializes various registers to predefined status.

This bit is set by BINIT, or by being set by the host processor.

The host should not write to this bit when it is already set.

Indirect Address Register Pointer - Bits <02:00>

Read/Write

These bits are used to select the desired channel register when accessing a block of indexed registers. These bits form the binary number of the channel to be accessed.

7.2.2 Receiver Buffer (RBUF) +2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DV	OE	PE	PER	0	Rx Line No.			Received Character							

Read Once, Word Addressable

This register has the same address as the Transmit Character Register (TXCHAR). However, a Read from 'base + 2' is interpreted by the controller hardware as a Read from the FIFO buffer. Therefore, RBUF is a 256-character register with a single-word address. The Least Significant Bit (LSB) of the character is in bit zero.

Data Valid (DV) - Bit 15

Read-Only

Cleared by Master Reset or by FIFO buffer becoming empty

This bit is set when the first character is loaded into the FIFO. This bit remains set as long as there is valid data in the FIFO buffer.

After self-test, diagnostic information is loaded into the FIFO buffer. Consequently, this bit is always set after a successful Master Reset sequence.

Overrun Error (OE) - Bit 14

Read-Only

This bit is set if one or more previous characters on the channel indicated by Rx Line Number (bits <11:08> were lost due to a full FIFO buffer, or the failure of the controller to service the DUARTs. (Also see Received Character, bits <07:00>).

NOTE

The 'all ones' code for bits <14:12> is reserved. This code indicates that modem status or diagnostic information is held in RBUF bits <07:00>.

Framing Error (FE) - Bit 13

Read-Only

This bit is set if the first stop bit of the received character was not detected. (Also see Received Character, bits <07:00>).

Parity Error (PER) - Bit 12

Read-Only

This bit is set if this character has a parity error and parity is enabled for the channel indicated by bits <11:08>. (Also see Received Character, bits <07:00>).

Receive Line Number - Bits <10:08>

These bits contain the number of the channel (in binary) on which the character of RBUF <07:00> was received or on which a data set change was reported.

Received Character - Bits <07:00>

Read-Only

If RBUF bits <14:12> equals 000, these eight bits contain the oldest character in the FIFO buffer. The character is good.

If RBUF bits <14:12> equals 001, 010, or 011, these eight bits contain the oldest character in the FIFO buffer. The character is bad.

If RBUF <14:12> equals 111, these eight bits contain diagnostic or modem status information. In this case, RBUF bit 00 has the following meanings:

0 = Modem status in RBUF (bits <07:01>) (see subsection 7.3.8.3).

1 = Diagnostic information in RBUF (bits <07:01>) (see subsection 7.3.5).

If there is an overrun condition, the DUART data buffer for that channel will be cleared. A null character, with OE (bit 14) set will be placed in the receive character FIFO buffer. The cleared data will be lost.

The controller does not have a break detect bit. A line break is indicated to the program as a null character with FE (bit 13) set.

7.2.3 Transmit Character Buffer (TXCHAR) +2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TDV	0	0	0	0	0	0	0	Transmit Character							

Write Only, Word Addressable
Indexed by Ind. Add. Reg.

Single-character programmed transfers are made via this register.

Transmit Data Valid (TDV) - Bit 15

Write-Only

When set, this bit instructs the controller to transmit the character held in bits <07:00>. This bit is sensed by the controller which then transfers the character, clears the bit and sets Transmitter Action (bit 15 in the CSR).

NOTE

TXCHAR contents should not be changed by read-modify-write instructions, such as BIS, BIC, INC, or DEC. These instructions may lose the state of the TDV bit.

Transmit Character - Bits <07:00>

Write-Only

These bits contain the character to be transmitted. The LSB is bit zero. For seven-, six- or five-bit characters, unused bits must be set to zero.

7.2.4 Line Parameter Register (LPR) +4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Tx Data Rate				Rx Data Rate				SC	EP	PE	Char. Length		Diag Code		0

Read/Write, Byte Addressable
Indexed by Ind. Add. Reg.

This register is used to configure its associated channel.

Transmitted Data Rate - Bits <15:12>

Read/Write

Set to 1101 (9600 bps) by Master Reset

These bits select the transmit data rate on a per channel basis (see Table 7-1).

Received Data Rate - Bits <11:08>

Read/Write

Set to 1101 (9600 bps) by Master Reset

These bits select the receive data rate on a per channel basis (see Table 7-1).

Stop Code (SC) - Bit 07

Read/Write

Cleared by Master Reset

This bit specifies the number of stop bits at the end of the character. The length is determined by setting the code as shown below:

0 = 1 stop bit for 5-, 6-, 7- or 8-bit characters
1 = 2 stop bits for 6-, 7- or 8-bit characters, or 1.5 stop bits for 5-bit characters

Table 7-1. Transmit and Receive Data Rates for the DHV11

Code	Data Rate	Group
0000	50	A
0001	75	B
0010	110	A and B
0011	134.5	A and B
0100	150	B
0101	300	A and B
0110	600	A and B
0111	1200	A and B
1000	1800[1]	B
1001	2000	B
1010	2400	A and B
1011	4800	A and B
1100	7200	A
1101	9600	A and B
1110	19200	B
1111	38400	A

[1] This speed may be affected by the CS08/E1 configuration program. See section 4.4 for details on nonstandard baud rate substitution.

NOTE

When split speed operation is used, the transmit and receive baud rates must be from the same group (A or B). If this rule is broken, both the transmission and reception for a channel will operate at the baud rate specified for reception.

All channels in the CS08/E1 are paired up: channels 0 and 1, 2 and 3, and so forth. The data rates for paired channels must be in the same group. For example, if channel 0 is set for 7200 baud (group A only) and channel 1 is subsequently set for 19200 baud (group B only), channel 0 will be automatically reset to 19200 baud.

Even Parity (EP) - Bit 06

Read/Write

Cleared by Master Reset

When PE (bit 05) is set, this bit controls the sense of parity as shown below:

0 = odd parity
1 = even parity

Parity Enable (PE) -Bit 05

Read/Write

Cleared by Master Reset

When set, this bit causes a parity bit to be generated and added on transmission, and checked and removed on reception for the selected channel.

Character Length - Bits <04:03>

Read/Write

Set to 11 by Master Reset

These bits define the character length, excluding the start, stop and parity bits. The character length is determined by setting the code as shown below.

00 = 5 bits per character
01 = 6 bits per character
10 = 7 bits per character
11 = 8 bits per character

Diagnostic Code - Bits <02:01>

Read/Write

Cleared by Master Reset

These bits enable the Background Monitor Program (BMP) for a line. Refer to section 7.3.7 for details of BMP operation.

00 = Normal operation
01 = Enables BMP

7.2.5 Line Status (STAT) +6

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DSR	0	RI	DCD	CTS	0	0	0	0	0	0	0	0	0	0	0

Read-Only, Byte Addressable
Indexed by Ind. Add. Reg.

The high byte of this register holds modem status information. The low byte is undefined.

Data Set Ready (DSR) - Bit 15

Read-Only

This bit indicates the current status of the Data Set Ready signal from the modem. The status of this bit is defined below.

1 = ON
0 = OFF

NOTE

To report a modem status change the controller writes the high byte of STAT into the low byte of RBUF and sets RBUF bits <14:12> equal to 111 to indicates that RBUF holds a modem signal change. See subsection 7.3.8.3.

Ring Indicator (RI) - Bit 13

Read-Only

This bit indicates the current status of the Ring Indicator signal from the modem. The status of this bit is defined below.

1 = ON
0 = OFF

Data Carrier Detected (DCD) - Bit 12

Read-Only

This bit indicates the current status of the Data Carrier Detected signal from the modem. The status of this bit is defined below.

1 = ON
0 = OFF

Clear To Send (CTS) - Bit 11

Read-Only

This bit indicates the current status of the Clear To Send signal from the modem. The status of this bit is defined below.

1 = ON
0 = OFF

7.2.6 Line Control Register (LNCTRL) +10

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	RTS	0	0	DTR	LT	Maint. Mode		FXO	OAF	BC	RE	IAF	TDA

Read/Write, Byte Addressable
Indexed by Ind. Add. Reg.

Request To Send (RTS) - Bit 12

Read/Write

Cleared by Master Reset

This bit controls the Request To Send signal. The status of this bit is defined below.

1 = ON
0 = OFF

Data Terminal Ready (DTR) - Bit 09

Read/Write

Cleared by Master Reset

This bit controls the Data Terminal Ready signal. The status of this bit is defined below.

1 = ON
0 = OFF

Link Type (LT) - Bit 08

Read/Write

Cleared by Master Reset

If the channel is connected to a modem, this bit must be set. When this bit is set, any change in modem status will be reported via the FIFO buffer and the STAT Register.

If this bit is reset, the channel becomes a 'data leads only' channel, and modem status information is loaded in the high byte of the STAT Register, but not placed in the FIFO buffer.

Maintenance Mode - Bits <07:06>

Read/Write

Cleared by Master Reset

These bits can be written by the driver or test programs in order to test the channel. The status of these bits is defined below.

00 = Normal operation

01 = Automatic Echo Mode -
Received data is retransmitted (regardless of the state of TE bit (bit 15 of TBUFFAD2) at the data rate selected for the receiver. The received characters are processed normally and placed in the received character FIFO buffer. In this mode, the controller will not transmit any characters (including internally-generated flow-control characters). The RE bit (bit 02) must be set when operating in this mode.

10 = Local (Internal) Loopback -
The DUART channel output is internally connected to the input. Normal received data is ignored and the transmit data line is held in the marking state. In this mode, flow-control characters will be looped back instead of being transmitted. The data rate selected is for the both the transmission and reception. The TE bit (bit 15 of TBUFFAD2) still controls transmission in this mode. Receiver Enable (bit 03) should be disabled prior to enabling or disabling the local loopback mode and re-enabled after the new mode has been selected.

11 = Remote Loopback -
In this mode received data is transmitted at the same speed it is received. The data is not placed in the receiver FIFO buffer. The state of TE (bit 15 of TBUFFAD2) is ignored.

Force X-Off (FXO) - Bit 05

Read/Write

Cleared by Master Reset

This bit can be set by the program to indicate that this channel is congested at the host system. When the controller sees this bit set, it will send an X-OFF code. Until this bit is reset, X-OFFs will be sent after every alternate character received on that channel. When this bit is reset, an X-ON will be sent unless IAF (bit 01) is set and the FIFO buffer is critical.

This operation of this bit may be affected by user-selected flow control options. See subsection 7.3.4 for further details.

Outgoing Auto Flow (OAF) - Bit 04

Read/Write

Cleared by Master Reset

This bit controls the auto-flow for outgoing characters. When this bit and RE (bit 02) is set, the controller will automatically respond to X-ON and X-OFF codes received from a channel. The controller uses the TE (bit 15 of TBUFFAD2) to terminate and initiate the flow.

This operation of this bit may be affected by user-selected flow control options. See subsection 7.3.4 for further details.

Break Control (BC) - Bit 03

Read/Write

Cleared by Master Reset

If set, this bit forces the selected channel to the Spacing state after the current character has been sent. Transmission resumes after the break has been cleared.

If the break timer option is enabled (see section 4.4), the duration of a break may be timed by transmitting characters in programmed I/O or DMA mode. The duration of each character is user-selectable. Use the following procedure:

1. Enable transmission.

2. Set the Break Control bit.

3. Transmit characters in either PIO or DMA mode. Interrupts must be enabled if you wish to be interrupted when the transmission is over. The length of the break (in milliseconds) is (break timer value) * (number of characters - 1).

4. Check the TA bit in the CSR.

5. Turn off the Break Control bit.

Receiver Enable (RE) - Bit 02

Read/Write

Cleared by Master Reset

When this bit is set, the receiver for the selected channel is enabled. If this bit is cleared while a character is being assembled, the character is lost.

Incoming Auto Flow (IAF) - Bit 01

Read/Write

Cleared by Master Reset

When set, this bit allows the controller to perform flow control for the selected channel by transmitting X-ON/X-OFF codes.

The controller will send an X-OFF character to channels when the receiver FIFO buffer becomes critically full. An X-ON character will be sent when it is considered congestion is no longer a problem.

This operation of this bit may be affected by user-selected flow control options. See subsection 7.3.4 for further details.

NOTE

An X-ON code = 21_8 = DC1 = CTRL/Q.
An X-OFF code = 23_8 = DC3 = CTRL/S.

No other codes are specified for the interface.

Transmit DMA Abort (TDA) - Bit 00

Read/Write

Cleared by Master Reset

This bit is set by the driver program to halt the transfer of a DMA buffer. The transfer can be continued by clearing this bit and then setting TDS (bit 07 of TBUFFAD2). No characters will be lost.

If this bit is not cleared before setting TDS, the transfer will be aborted before any characters are transmitted. See also, subsection 7.3.8.1.

7.2.7 Transmit Buffer Address 1 (TBUFFAD1) +12

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Buffer Address -- Least Significant Part															

Read/Write, Word Addressable
Indexed by Ind. Add. Reg.
Cleared by Master Reset

These bits are bits <15:00> of the DMA address.

Prior to a DMA transfer these 16 bits and the low byte of TBUFFAD2 are loaded by the host with the start address of the DMA buffer. This address is invalid during a DMA transfer. When TA (bit 15 of the CSR) is returned, the address will be valid.

7.2.8 Transmit Buffer Address 2 (TBUFFAD2) +14

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TE	0	0	0	0	0	0	0	TDS	0	Tx Buffer Address					

Read/Write, Byte Addressable
Indexed by Ind. Add. Reg.

Transmitter Enable (TE) - Bit 15

Read/Write

Set by Master Reset

When this bit is set, the controller will transmit all characters. When this bit is cleared, the controller will transmit only internally-generated flow-control characters.

In the Outgoing Auto-Flow mode, this bit is used by the controller to control outgoing characters. See also, subsection 7.3.4.

Transmit DMA Start (TDS) - Bit 07

Read/Write

Cleared by Master Reset

This bit is set by the CPU to initiate a DMA transfer. The controller will reset this bit prior to returning TA (bit 15 of the CSR).

NOTE

After setting this bit, the CPU must not write to TBUFFCT, TBUFFAD1 or bits <07:00> of TBUFFAD2 until TA report has been returned.

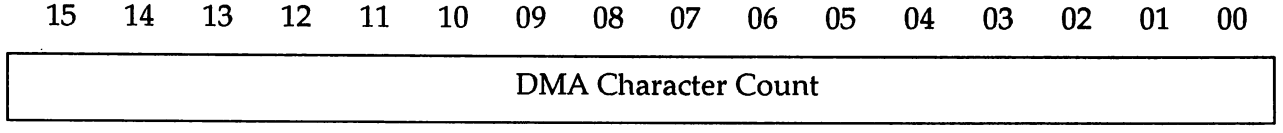
Transmit Buffer Address (TBA) - Bits <05:00>

Cleared by Master Reset

These bits are bits <21:16> of the DMA address.

Prior to a DMA transfer the low byte of this register and all 16 bits of TBUFFAD1 are loaded by the CPU with the start address of the DMA buffer. This address is invalid during a DMA transfer. When TA (bit 15 of the CSR) is returned, the address will be valid.

7.2.9 Transmit DMA Buffer Count (TBUFFCT) +16



Read/Write, Word Addressable
Indexed by Ind. Add. Reg.

These read/write bits are loaded with the number of characters to be transferred by DMA. The number of characters is specified as a 16-bit unsigned integer. After a DMA transfer has been aborted, this location will hold the number of characters still to be transferred.

After TDS (bit 07 of TBUFFAD2) has been set, this register must not be written to until the TA report has been returned.

7.3 DHV11 General Programming Information

7.3.1 Initialize

After a bus reset, or when the CPU sets Master Reset (bit 05 of CSR), the controller runs a self-test and initializes itself.

Following a successful self-test, eight diagnostic codes are placed in the FIFO buffer (see subsection 7.3.5) and the Diagnostic Fail bit (bit 13 of the CSR) and the Master Reset bit are reset. The self-test can be skipped if desired (see section 7.3.5.3).

After a successful initialization, the channels and registers are set as shown in the Table 7-2.

Table 7-2. Default Line and Register Values

Line Characteristic	Setting
Baud Rate	9600
Number of Data Bits	Eight
Number of Stop Bits	One
Parity	No
Parity Type	Odd
Auto-Flow	Off
Reception	Disabled
Transmission	Enabled
Register	**Value**
CSR	000220
RBUF	170201
LPR	156430
STAT	0 (unless modem signals are present)
LNCTRL	0
TBUFFAD1	0
TBUFFAD2	100000
TBUFFCT	0

7.3.2 Programmable Parameters

Following the controller's self-initialization, the driver program can configure the controller as needed. The configuration is accomplished via the LPR and LNCTRL registers.

Selectable parameters for each channel include:

- data rate
- character length
- parity
- stop bit length

Also, auto-flow can be selected, and individual receivers and transmitters can be enabled.

For operation with devices using modem-type signals, LT of the associated LNCTRL register should be set.

NOTE

If RE is reset while a receive character is being assembled, that character will be lost.

7.3.3 Interrupts

There are two types of interrupts: transmit and receive. Each type is described below.

Transmitter Action (CSR bit 15). This bit is set by the controller when any of four possible conditions occur. Those conditions are:

1. the last character of a DMA buffer leaves the DUART.
2. a DMA transfer is aborted.
3. a DMA transfer is terminated because of a non-existent memory being addressed or because of a memory parity error (either case causes TDE to be set).
4. a single-character programmed output is accepted.

Receive Data Available (CSR bit 07). This bit is set by the controller when a received character, or modem status, or diagnostic information is available in the FIFO buffer.

7.3.4 Data Flow Control

Data flow on communications devices is commonly controlled with X-ON and X-OFF codes. However, to make use of these codes, interfaces must have suitable decoding hardware or software.

A channel which receives an X-OFF character stops transmitting data until it receives an X-ON character. A channel which is becoming overrun by received data sends an X-OFF character. When congestion is relieved, it sends an X-ON character.

If the controller is programmed for automatic flow control (Auto-Flow), it can automatically control the flow of characters. The three bits which control the flow are IAF, FXO and OAF (LNCTRL bits 01, 05 and 04, respectively). IAF and FXO control incoming characters. IAF is an enable bit which allows the state of the FIFO buffer counters to control the generation of X-ON and X-OFF characters. The FXO bit is a direct command from the program.

Characteristics of auto-flow are listed below:

1. The controller hardware recognizes a three-quarters full and a half full FIFO buffer. The firmware uses this recognition to initiate auto-flow control procedures.

   If the program sets a channel's IAF bit, the controller will send that channel an X-OFF character if it receives a character after the FIFO buffer becomes three-quarters full. Should the channel fail to respond to the X-OFF, the controller will send an X-OFF in response to every character received unless it is an X-OFF. An X-ON character will be sent when the FIFO buffer becomes less the half full, unless FXO is set for that channel. X-ONs are sent only to channels to which an X-OFF has been sent.

   The program can perform flow control directly by inserting X-ON and X-OFF characters into the data stream. If the controller is in the IAF mode though, the results will be unpredictable.

   In the IAF mode, if RE (LNCTRL bit 02) is set, X-ONs and X-OFFs will be sent even if TE (TBUFFAD2 bit 15) is cleared.

2. When FXO is set, the controller sends an X-OFF and then acts as though IAF is set and the FIFO buffer is three-quarters full and is not yet less than half full. When FXO is reset, an X-ON character will be sent unless the FIFO buffer is critically full and IAF is set.

3. If the program sets OAF, the controller will automatically respond to X-ON and X-OFF characters from the channel. It does this by setting and clearing the TE bit.

   The program may also control the TE bit. Consequently, it is important to keep track of received X-ON and X-OFF characters.

Received X-ON and X-OFF characters will always be reported via the FIFO buffer. It is possible during read-modify-write operations by the program for the controller to alter the state of TE between the read and the write action. Therefore, if DMA transfers are initiated while while IAF is set, only the low byte of TBUFFAD2 should be written to.

The controller may change the state of TE for up to 20 microseconds after OAF is cleared by the program.

When checking for flow-control characters, the controller only checks characters which contain no transmission errors. The parity bit is stripped and the remaining bits are checked for X-ON and X-OFF characters.

Data flow control can be modified by user-selectable flow control options. See section 4.5.8 for further details.

7.3.5 Diagnostic Codes

7.3.5.1 Self-Test Diagnostic Codes

After bus reset or master reset, the controller executes a self-test and initialization sequence. At the end of the sequence, eight diagnostic codes are put in the FIFO buffer. RDA is set and the Master Reset bit is cleared.

If an error is detected during the test, DF (CSR bit 13) is set, and the Fault LED will be ON. After an error-free test, DF is reset, and the Fault LED will be OFF.

7.3.5.2 Interpretation of Self-Test Codes

The high byte of RBUF can be interpreted as described in subsection 7.2.2, except that bits <11:08> are not the line number. Instead, they represent the sequence of the diagnostic byte, where zero equals the first byte, one equals the second byte, and so on.

Table 7-3 shows the interpretation of the diagnostic code for the low byte of RBUF. Table 7-4 lists the self-test error codes.

NOTE

The error code definitions make references to 'processor 1' (PROC1) and 'processor 2' (PROC2), which refer to the two processors on the DEC DHV11. The CS08/E1 actually contains only one processor. The code references to two processors were emulated to maintain full diagnostic compatibility with the DEC DHV11. This includes the ROM version codes which refer to ROM versions in the DEC DHV11. Codes not defined in Table 7-4 indicate undefined errors.

Table 7-3. DHV11 Self-Test Diagnostic Codes

Bit	Status Indication
00	0 indicates modem status 1 indicates diagnostic code
01	If bit 07 equals one, then: 0 indicates PROC1-specific errors in bits <04:02> 1 indicates PROC2-specific errors in bits <04:02>
02 03 04 05	Used to define codes (see Table 7-4)
06	If bit 07 equals one, then: 0 indicates self-test code in bits <05:01> 1 indicates BMP code in bits <05:01>
07	If bit 00 equals one, then zero in bit 07 indicates ROM version in bits <06:02> and bit 01 is the PROC number. 1 indicates diagnostic code in bits <06:01>
PROC1 = processor 1 PROC2 = processor 2	

Table 7-4. DHV11 Self-Test Error Codes

RBUF Low Byte								Octal	
07	06	05	04	03	02	01	00	Code	Code Description
1	0	0	0	0	0	0	1	201	Self-Test null code (used as filler)
1	0	0	0	0	0	1	1	203	Self-Test skipped
1	0	0	0	1	0	0	1	211	Basic data path error from PROC2
1	0	0	0	1	0	1	1	213	Undefined DUART error
1	0	0	0	1	1	1	1	217	Received character FIFO, logic error
1	0	0	1	0	1	0	1	225	PROC1 to common RAM error
1	0	0	1	0	1	1	1	227	PROC2 to common RAM error
1	0	0	1	1	0	0	1	231	PROC1 internal RAM error
1	0	0	1	1	0	1	1	233	PROC2 internal RAM error
1	0	0	1	1	1	0	1	235	PROC1 ROM error
1	0	0	1	1	1	1	1	237	PROC2 ROM error
PROC1 = processor 1 PROC2 = processor 2									

After self-test, the eight codes in the FIFO buffer will consist of six diagnostic codes and two ROM version codes. If there are less than six error codes to report, null codes (201_8) fill the unused places.

If self-test is skipped (see subsection 7.3.5.3), six 203_8 codes and two ROM version codes will be returned.

7.3.5.3 Skipping Self-Test

The self-test takes up to 2.5 seconds to complete. This may cause up to a 2.5 second hang-up, depending on the system software. Self-test may be skipped by using the procedure below.

1. The program resets the controller.

2. The diagnostic firmware writes 125252_8 throughout the common RAM, within eight milliseconds (ms) of reset.

3. The program waits 10 ms (+ or - 1 ms) after issuing reset. It then writes 052525_8 throughout the control registers (except the CSR), within the next four ms.

4. The diagnostic firmware waits until 16 ms after reset. It then checks for a 052525_8 code in common RAM.

   If it finds the code, self-test is skipped. The DF bit is cleared and control is passed to the communications firmware, which starts initialization.

   If the code is not found, self-test begins.

NOTE

The program must not write to the CSR or the control registers during the period starting 15 ms after reset, and ending when the Master Reset bit is cleared. This could cause a diagnostic fail condition.

7.3.6 Error Indication

Four bits are used to inform the program of transmission and reception errors. The four bits are listed below:

1. TDE - (CSR bit 12) (see subsection 7.2.1)
2. PER - (RBUF bit 12) (see subsection 7.2.2)
3. FE - (RBUF bit 13) (see subsection 7.2.2)
4. OE - (RBUF bit 14) (see subsection 7.2.2)

RBUF bits <14:12> are also used to identify modem status or diagnostic information.

7.3.7 Background Monitor Program

BMP is a firmware diagnostic program that reports controller errors. When it detects an error, it places a word in the receive FIFO that indicates the current status of the controller. In the low byte, 305_8 = controller running and 307_8 = controller error detected. In the high byte, line number = 0 and OE, PE, and PER are all set. If the error clears and then recurs, BMP places the diagnostic word in the FIFO each time the error recurs.

BMP can be enabled under software control by setting LPR bits <02:01>. In this case, it returns the line number of the LPR that was used. BMP clears bits <02:01> when it is finished. The host should not write to the LPR until these bits are cleared.

7.3.8 Receiver Operation

7.3.8.1 Receiver Scanner

The receiver section of each DUART is serviced by a receiver scanner which polls the DUARTs for a channel which has assembled a received character. Each of the two channels in the DUART has a receive character first-in-first-out (FIFO) buffer which is four deep. The received characters are tagged with the channel number and DV (bit 15 of RBUF) and are transferred to the FIFO, if it is not full. When a character is put in the RBUF FIFO the controller sets RDA (bit 07 of CSR). It remains set as long as valid data is held in RBUF. If RIE (bit 06 of CSR) is set, the program will be interrupted at the receive vector. The receiver interrupt routine should read RBUF until DV is reset. The receiver scanner has priority over the transmitter scanner because the transmit operation is by means of DMA or single-character transmission and can be deferred if necessary during conditions of peak activity. In this manner, characters are not lost and no overrun conditions are generated because of the operation of the controller itself.

7.3.8.2 FIFO Buffer Operation

The FIFO buffer is contained in the RAM memory. A 16-bit wide by 256-word deep FIFO storage is maintained by the controller's microprogram. In effect, a 16-bit word entered at the top of the FIFO buffer is automatically shifted down to the lowest location that does not already contain an entry. The bottom of the FIFO buffer is the Receiver Buffer Register (see subsection 7.2.2). RBUF is a read-once register: reading RBUF extracts the character and its associated status from the buffer and causes all other entries to shift down one position.

7.3.8.3 Half-Duplex Operation

When half-duplex operation is desired for a channel, the receiver must be blinded (disabled) from receiving the characters during transmission, if the transmitting is done on the same transmission line as the receiving. The program does this by resetting bit 02 of the Line Control Register for that line.

7.3.9 Transmitter Operation

Each channel of the controller can be programmed to transmit blocks of characters by Direct Memory Access (DMA), or single-characters only. The following subsections describe each type.

7.3.9.1 DMA Transmission

Unlike the receiver operation where the controller transfers received characters from the DUART to the FIFO for programmed input by the CPU, the CS08/E1 performs automatic direct memory access (DMA) of characters to be transmitted. Data is accessed a word at a time from the memory, except for odd bytes at the beginning or end of the buffer. The low-order byte is transferred to the DUART's transmitter-holding buffer, and the high-order byte is held in the controller's memory.

Prior to setting up a transfer of a DMA buffer, the program should make sure that TDS (bits <05:00> of TBUFFAD2) is not set. TBUFFCT, TBUFFAD1 and TBUFFAD2 should not be written to unless TDS is clear. Transmission will begin when the program sets TDS.

The size of the DMA buffer and its start address can be written to TBUFFCT, TBUFFAD1 and TBUFFAD2 in any order. Since TBUFFAD2 contains TE (bit 15) and TDS, it is probably simpler to write TBUFFAD2 last. By using byte operations on TBUFFAD2, setting TE and TDS can be separated.

The controller will perform the transfer and set TA (bit 15 of CSR) when it is complete. If TIE (bit 14 of CSR) is set, the program will be interrupted at the transmit vector.

To abort a DMA transfer, the program must set TDA (bit 00 of LNCTRL). The controller will halt transmission and update TBUFFCT, TBUFFAD1 and TBUFFAD2 (bit <07:00>) to reflect the number of characters which have been transmitted. TDS will then be cleared and TA set. If the interrupt is enabled, TA will interrupt the program at the transmit vector. If the program clears TDA and sets TDS, the transfer can be continued without loss of characters.

If a DMA transfer fails because of a memory error, the transmission will be terminated. TBUFFAD1 and TBUFFAD2 will point to the failing location and TBUFFCT will be cleared.

7.3.9.2 Single Character Transmission

Single characters are transferred via a channel's TXCHAR register. The character and the DV bit can be written together, or as separate MOVB instructions.

The controller returns TA when it reads the character from TXCHAR. As with DMA transfers, TA can be sensed via interrupt or by polling the CSR.

In single-character mode TA is returned when the controller accepts the character, **not** when it has been transmitted. Each channel has a three-character buffer. Therefore, if the modem status bits or line parameters are changed immediately after the last TA of a message, the end of the message could be lost. The program can prevent such a loss by adding three null characters to the end of each single-character programmed transfer message.

7.3.9.3 Modem Control

The CP08/M provides level conversion for modem control channels. The output control functions are RTS and DTR. The input control functions are: CTS, DSR, CD and RING.

CTS, DSR and CD are sampled by the microprogram every 10 ms. Therefore, for a change to be detected, these bits must stay steady for at least 10 ms after a change. RING is also sampled every 10 ms, but a change is not reported unless the new state is held for three consecutive samples. There are no hardware controls between the modem control logic and the receiver/transmitter logic. Any coordination should be done under program control. Modem status change reports placed in the received character FIFO buffer are positioned relative to the received characters.

A channel can be selected for modem operation by setting LT (LNCTRL bit 08). Any change of the modem status inputs will be reported to the program via the FIFO buffer and the STAT Register. Modem control bits must be driven by the program's communication routines. Control bits are written to LNCTRL.

A channel is selected as a 'data lines only' channel by resetting LT. Modem control and status bits can still be managed by the program but status bits must be polled at the high byte of the STAT Register. Changes of modem status will not be reported to the program via the FIFO.

NOTE

When transmitting by the single-character PIO method, up to three characters can be buffered in the controller hardware. If modem control bits are to be changed at the end of a transmission, three null characters should be added. When TA is set after the third null character, the last true character has left the DUART.

Status change reporting is done via the FIFO buffer. When OE, FE and PER are all set, the eight low-order bits contain either status change or diagnostic information. In addition:

- If RBUF bit 00 equals zero, RBUF bits <07:01> hold STAT bits <15:09> (see subsection 7.2.5).
- If RBUF bit 00 equals one, RBUF bits <07:00> hold diagnostic information (see subsection 7.3.5).

7.4 CC08 Controller Architecture

Figure 7-2 is a block diagram that shows the major functional elements of the CC08 Controller. The controller is organized around an eight-bit high-speed microprocessor which performs all controller functions. The ALU and register file portion of the microprocessor are implemented with two 2901 bit-slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with six 2K x 8-bit PROMs.

A 2K x 8-bit high-speed random access memory (RAM) holds the contents of device registers, silo buffer and working storage for the microprocessor. The RAM is both a source and destination to the internal data bus and is addressed directly and indirectly by the microprocessor.

The LSI-11 Bus interface consists of 42 bi-directional and two uni-directional signals. The LSI-11 Bus interface is used for programmed I/O, CPU interrupts and DMA Data Transfer operations. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA Read operations.

Because of the architecture of the CS08/E1, software drivers are typically interrupt driven. Rapid polling severely degrades the performance of the controller.

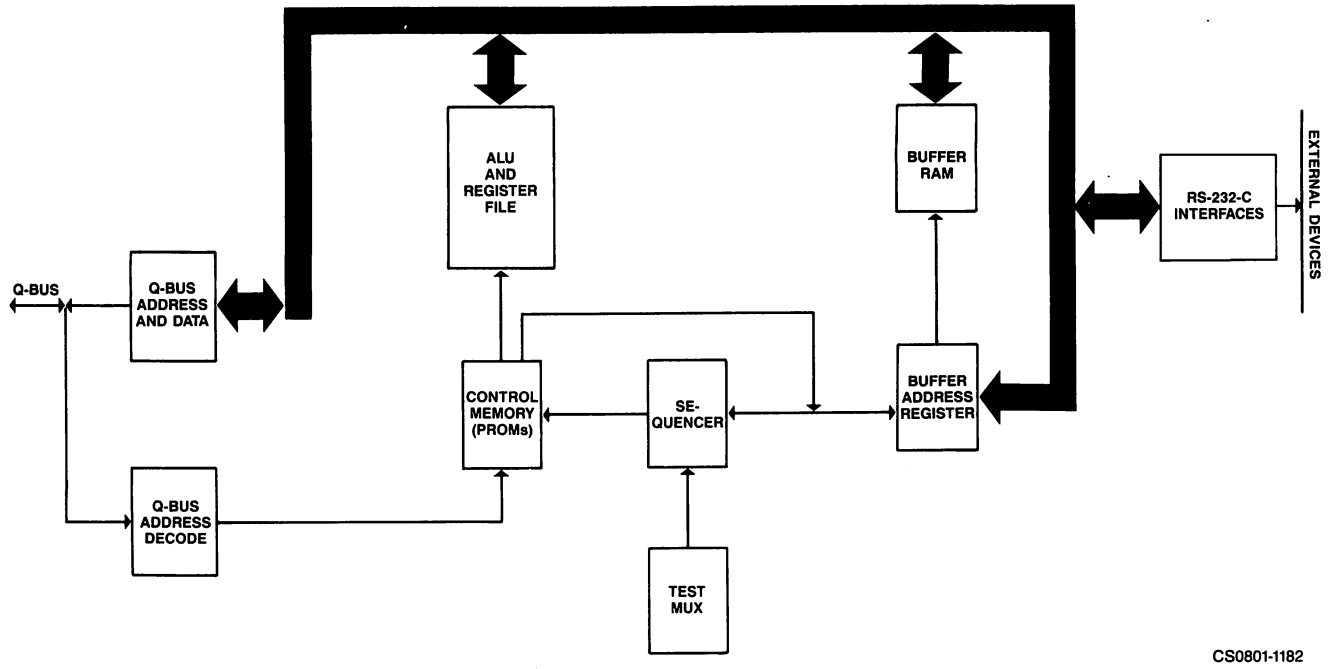


Figure 7-2. CC08 Controller Module Block Diagram

7.4.1 Receiver Operation

Reception on each channel is by means of Dual Universal Asynchronous Receiver/Transmitters (DUARTs). These MOS/LSI devices perform all the functions of double buffered asynchronous character assembly. The receiver section of the DUART samples the channel at 16 times the bit rate of the signals to be received on the channel. Upon detection of a mark-to-space transition, the DUART counts eight clock pulses and checks the state of the channel again. This sampling occurs in the center of the normal start bit. If the sample is a mark, the receiver returns to its idling state, ready to detect another mark-to-space transition. If the sample is a space, the receiver enters the data entry condition and samples the state of the channel at subsequent sample points spaced at multiples of 16 clock pulses from the center of the start bit. The number of samples taken is determined by the character length information and parity enable programmed in the device registers. If parity checking is enabled for the channel, the receiver computes the parity of the character received and compares it with the parity sense specified for reception on that channel. If the parity does not check, the parity error bit is set.

The character length, parity, and number of stop bits that are used by the DUART to perform the above operations are stored in each DUART from information received from the device register controlling the line parameters for the associated channel in the DUART.

7.4.2 Transmitter Operation

Transmission on each channel is also performed by DUARTs. These MOS/LSI devices perform all the necessary functions for double buffered asynchronous character transmission. The transmitter section of the DUART holds the serial output at a marking state when idle. When a character has been loaded into the transmitter-holding buffer, the DUART generates a start bit within 1/16 of the bit time. The start space is followed by five, six, seven, or eight data bits and the parity bit if parity is selected. Control of the DUART is performed by the device register controlling the line parameters. Data bits are presented to the channel with the least significant bit first.

If the transmitter's holding register has been loaded while a character is being transmitted, the start bit of the second character is transmitted immediately at the end of the preceding character's stop bits.

Appendix A
CABLE SCHEMATICS

A.1 Overview

This appendix contains diagrams of a variety of different cables used by the CS08/E1 subsystem. Many of these cables are available from Emulex (see Table 1-2 for part numbers). The following cables are shown in this appendix:

Figure	Cable Name	Description
A-1	Terminal Cable (25-pin to 25-pin)	This cable is used with the CP08/M for simple terminal hookups in which modem signals are not needed.
A-2	Terminal Cable (RJ11 to RJ11)	This cable is used with the CP08/J for simple terminal hookups in which modem signals are not needed.
A-3	RJ11 to DB25S	This connector attaches to the back of a terminal and enables use of the terminal cable (A-2).
A-4	Modem Cable	This cable connects a CP08/M port to a modem.
A-5	Null-Modem Cable	This cable is used when modem signals are required but the external device is connected directly to the CP08/M.
A-6	Level Flow Control Cable	This cable is used to connect devices to CP08/M ports configured for Emulex level flow control (see section 4.4.8).
A-7	Wraparound CP08/M	This is not a cable, just a 25-pin connector strapped to loop back signals. It is used during diagnostic testing of the CP08/M.
A-8	Wraparound CP08/J	This is an RJ12 connector strapped to loop back signals. It is used during diagnostic testing of the CP08/J.
A-9	Staggered Loopback (25-pin)	This cable is used in some diagnostic tests. It is similar to a wraparound but loops signals from one CP08/M port to another instead of directly back to the same port.
A-10	Staggered Loopback (RJ11 or RJ12)	This cable is used in some diagnostic tests. It is similar to a wraparound but loops signals from one CP08/J port to another instead of directly back to the same port.

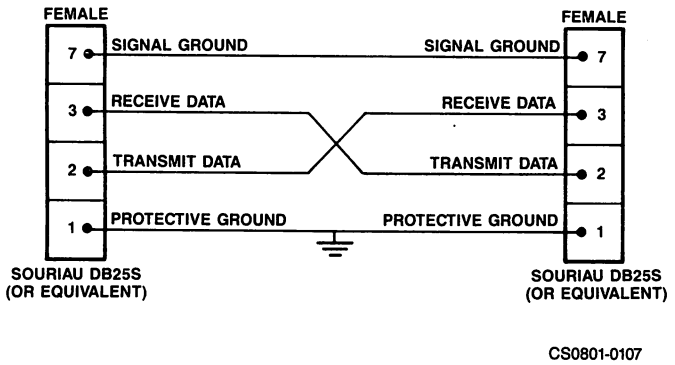


Figure A-1. Terminal Cable (25-pin to 25-pin)

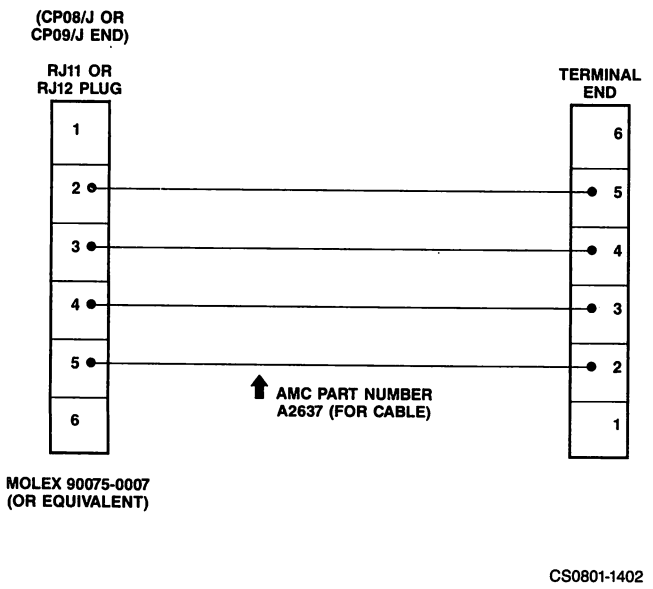


Figure A-2. Terminal Cable (RJ11 to RJ11)

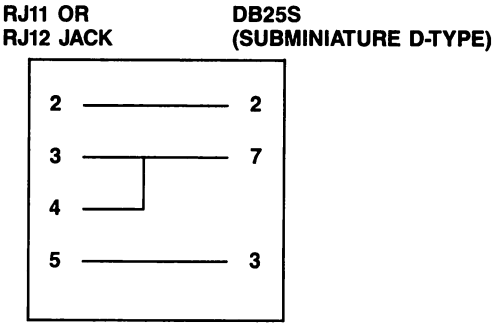


Figure A-3. RJ11 to DB25S

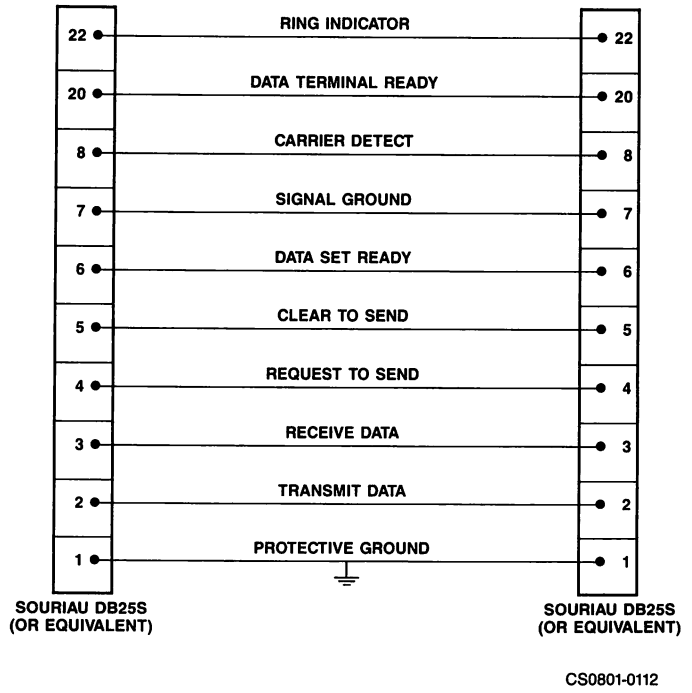


Figure A-4. Modem Cable

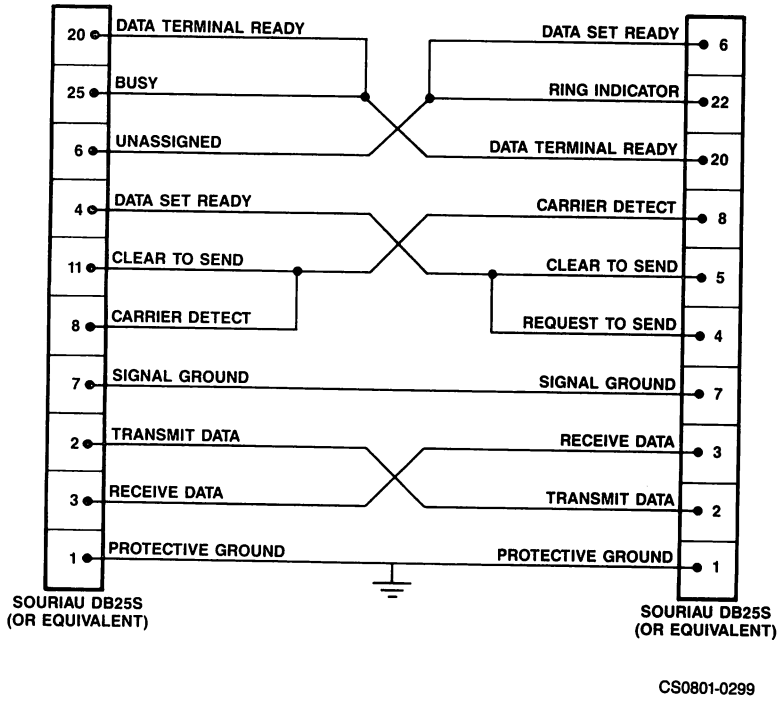


Figure A-5. Null-Modem Cable

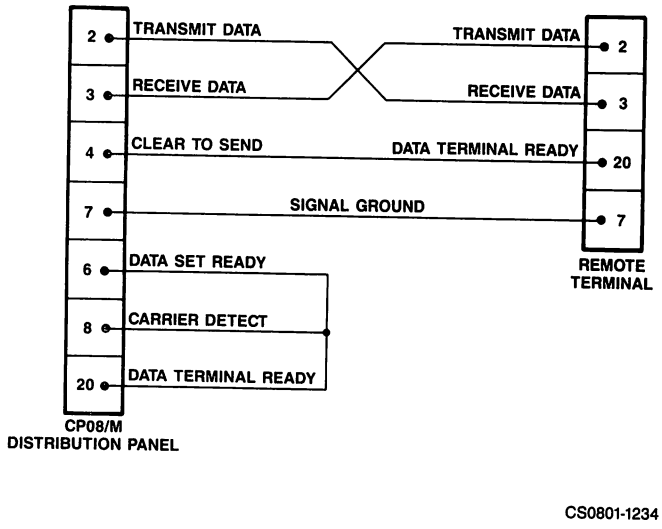


Figure A-6. Terminal Cable for Ports Using Level Flow Control

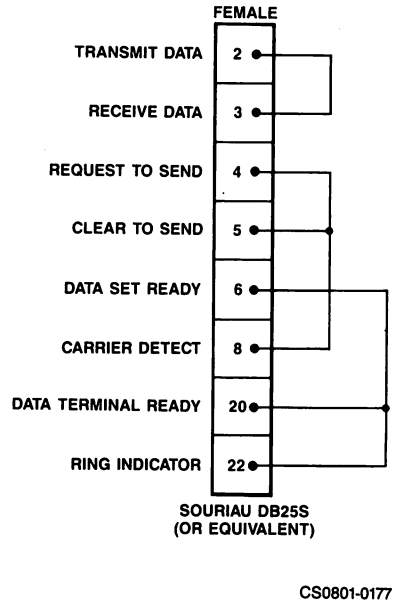


Figure A-7. Wraparound CP08/M

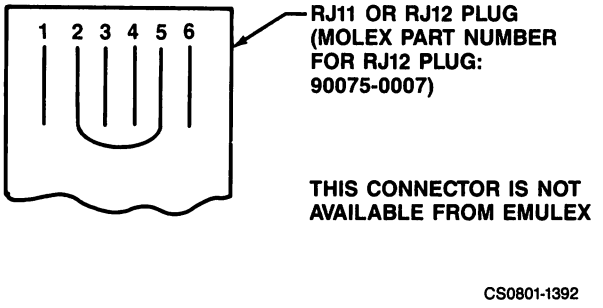


Figure A-8. Wraparound CP08/J

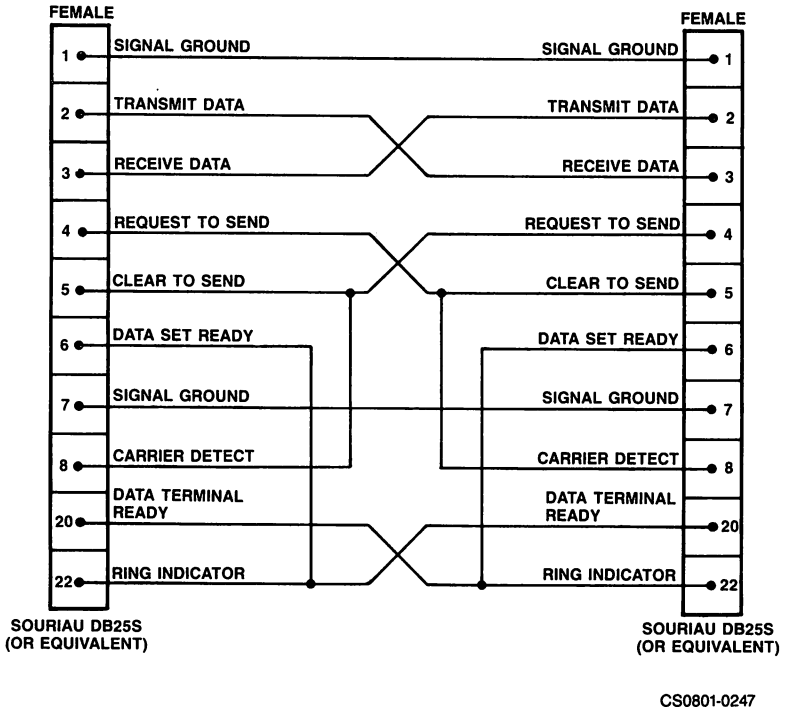


Figure A-9. Staggered Loopback CP08/M

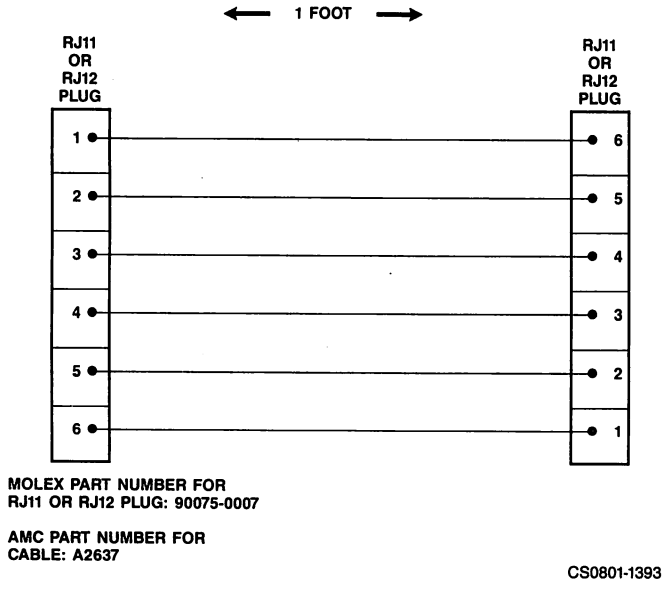


Figure A-10. Staggered Loopback CP08/J

Appendix B
ASSIGNING BUS AND VECTOR ADDRESSES

B.1 Overview

A host operating system must know what devices are attached to the bus if it is to make use of them. One way to get this information is to ask the user. If this procedure is used, the user assigns bus and vector addresses and enters this information during the SYSGEN process. The CPU then looks for devices at the addresses it was told it would find them. If you use this method, skip this appendix.

Another way to get this information is for the operating system to poll the bus when the system is bootstrapped to find out what is there. The DEC routine which does this polling is called autoconfigure and it is the subject of this appendix. Autoconfigure works this way: DEC has compiled a list of all devices with floating addresses supported by its operating systems (Table B-1). The autoconfigure routine starts by searching for the first device on the list (DJ11). If it finds one, it assigns it an address. Then it searches for the next device and continues until it has searched for the last device on the list. When it is done, it has searched for every device that DEC supports and has assigned an address to all the devices it has found. The autoconfigure routine also assigns interrupt vector addresses, but note that the order in which it assigns vector addresses is different from bus addresses. Table B-2 shows the search order for vector addresses.

Because of the nature of this routine, the address assigned to a device depends on what other devices are on the system. If a new device is added to the system, every device which comes after it on one of the lists will be moved up and assigned a higher address than it had before. (Keep in mind, however, that because the order of the lists is different a device might get moved up on the bus address list and still keep its old vector address, or vice versa. One address does not have to change simply because the other one did.)

NOTE

Some DEC devices have fixed bus and vector addresses. These devices will not be found on the search list and their addresses will not change when other devices are added to the system. For the purposes of assigning floating bus and vector addresses, these devices can be ignored.

The operating system expects to find a device at whatever address it assigned to it during the autoconfigure process. Therefore, whatever addresses it assigned to that device must by physically programmed into the device before the system is brought on line. If this is not done, the system will hang because the CPU will look for the device at the address assigned to it but the device will not respond. If you choose the autoconfigure option during SYSGEN, you must be careful to

calculate the exact bus and address vectors that will be assigned during the autoconfigure process.

So, before you install the CS08/E1, you must:

- Calculate the address the DEC autoconfigure routine is going to assign it,
- Figure out if the addresses for any of the other devices on your system are going to change, and
- Make sure these addresses are programmed correctly into the devices.

In the case of the CS08/E1, the bus and vector addresses are programmed via the configuration program (as described in Section 4). If the addresses of any of your other devices are going to change, you must also program the new addresses into them, as described in their technical manuals.

When calculating the bus and vector addresses, keep in mind that the CS08/E1 emulates a single DHV11.

B.2 Calculating Bus and Vector Addresses

There are two ways bus and vector addresses can be calculated:

- If you are using a MicroVAX under MicroVMS, use the CONFIGURE command. With this command, you simply list the devices in your system and MicroVMS figures out the correct bus and vector address for you. The CONFIGURE command is described in section B.2.1
- If you are using any other operating system, you will have to calculate bus and vector addresses manually. This is described in sections B.2.2 and B.2.3.

B.2.1 Using the MicroVMS CONFIGURE Command

The following procedure tells how to use the MicroVMS CONFIGURE command to determine LSI-11 bus addresses and interrupt vectors:

1. Login to the system manager's account. Run the SYSGEN utility:

   $ RUN SYS$SYSTEM:SYSGEN<return>
   SYSGEN>

   The SYSGEN> prompt indicates that the utility is ready to accept commands.

```
Name: MSA Units: 1 Nexus: 0  CSR: 772520  Vector1: 224  Vector2: 000
Name: PUA Units: 1 Nexus: 0  CSR: 772150  Vector1: 154  Vector2: 000
Name: PUB Units: 1 Nexus: 0  CSR: 760334* Vector1: 300  Vector2: 000
Name: TXA Units: 1 Nexus: 0  CSR: 760500* Vector1: 310* Vector2: 000

*Floating address or vector
```

Figure B-1. Sample SHOW CONFIGURATION

2. Obtain a list of devices already installed by typing:

   SYSGEN> **SHOW/CONFIGURATION<return>**

   SYSGEN lists by logical name the devices already installed on the LSI-11 Bus. Make a note of the other devices with floating addresses (greater than 760000_8) or floating vectors (greater than 300_8) that you plan to re-install with your CS08/E1.

   The example in Figure B-1 illustrates a SHOW/CONFIGURATION listing on a system with one TS11 tape controller, two MSCP disk controllers, and one DHV11 communications controller.

3. Execute the CONFIGURE command:

   SYSGEN> **CONFIGURE<return>**
   DEVICE>

   Specify the LSI-11 bus devices to be installed by typing their LSI-11 bus names at the DEVICE prompt. The CS08/E1 emulates one DHV11s, so enter a total of two DHV11s:

   DEVICE> **TS11<return>**
   DEVICE> **UDA,2<return>**
   DEVICE> **DHV11,2<return>**

   A comma separates the device name from the number of devices of that type to be installed. The number of devices is specified in decimal.

   In addition to the CS08/E1, you need only specify devices that have floating addresses or vectors. Devices with fixed addresses or vectors do not affect the address or vector assignments of devices with floating addresses and vectors.

```
SYSGEN>  CONFIGURE
DEVICE> TS11
DEVICE> UDA,2
DEVICE> DHV11,3
DEVICE> ^Z
Device: TS11    Name: MSA  CSR: 772520   Vector: 224   Support: yes
Device: UDA     Name: PUA  CSR: 772150   Vector: 154   Support: yes
Device: UDA     Name: PUB  CSR: 760334*  Vector: 300*  Support: yes
Device: DHV11   Name: TXA  CSR: 760500*  Vector: 310*  Support: yes
Device: DHV11   Name: TXB  CSR: 760520*  Vector: 320*  Support: yes

*Floating address or vector
```

Figure B-2. CONFIGURE Command Listing

4. Indicate that all devices have been entered by pressing the <ctrl> and Z keys simultaneously:

   DEVICE> ^Z

   SYSGEN lists the addresses and vectors of the devices entered in the format shown in Figure B-2.

5. Note down the CSR addresses and program them into non-Emulex controllers as instructed by the manufacturer and into the CS08/E1 as described in Section 4.

B.2.2 Calculating the Bus Address Manually

The bus address for a floating-address device is selected according to the algorithm used during autoconfigure. The algorithm is used in conjunction with a SYSGEN Device Table, Table B-1. Floating bus addresses start at 760010 and go up sequentially.

There are four rules that pertain to the assignment of bus addresses in floating address space:

1. Devices with floating addresses must be attached in the order in which they are listed in Table B-1. That is, a device higher on the list will always have a higher bus address.

Table B-1. SYSGEN Device Table

Rank	Device	Number of Registers	Octal Modulus	Rank	Device	Number of Registers	Octal Modulus
1	DJ11	4	10	16	KW11-C	4	10
2	DH11	8	20	17	Reserved	4	10
3	DQ11	4	10	18	RX11[2]	4	10
4	DU11,DUV11	4	10	18	RX211[2]	4	10
5	DUP11	4	10	18	RXV11[2]	4	10
6	LK11A	4	10	18	RXV21[2]	4	10
7	DMC11	4	10	19	DR11-W	4	10
7	DMR11	4	10	20	DR11-B[3]	4	10
8	DZ11[1]	4	10	21	DMP11	4	10
8	DZV11	4	10	22	DPV11	4	10
8	DZS11	4	10	23	ISB11	4	10
8	DZ32	4	10	24	DMV11	8	20
9	KMC11	4	10	25	DEUNA[2]	4	10
10	LPP11	4	10	26	UDA50[2]	2	4
11	VMV21	4	10	27	DMF32	16	40
12	VMV31	8	20	28	KMS11	6	20
13	DWR70	4	10	29	VS100	8	20
14	RL11[2]	4	10	30	Reserved	2	4
14	RLV11[2]	4	10	31	KMV11	8	20
15	LPA11-K[2]	8	20	**32**	**DHV11**	**8**	**20**

[1] DZ11-E and DZ11-F are treated as two DZ11s.
[2] The first device of this type has a fixed address. Any extra devices have a floating address.
[3] The first two devices of this type have a fixed address. Any extra devices have a floating address.

2. The bus address for a given device type is assigned on boundaries according to the number of registers that the device has. The boundaries are shown in the Octal Modulus column of Table B-1. The following table relates the number of device registers to possible boundaries.

Device Registers	Possible Boundaries
1	Any Word
2	XXXXX0, XXXXX4
3,4	XXXXX0
5,6,7,8	XXXX00, XXXX20, XXXX40, XXXX60
9 thru 16	XXXX00, XXXX40

3. A gap of at least eight-bytes must follow the register block of any installed device to indicate that there are no more of that type of device. This gap must start on the proper boundary for that type of device.

4. An eight-byte gap must be reserved in floating address space for each device type that is not installed in the current system. The gap must start on the proper boundary for the type of device the gap represents. That is, a single DJ11 installed at 760010 would be followed by a gap starting at 760020 to show a change of device types. A gap to show that there are none of the next device on the list, a DH11, would begin at 760040, the next legal boundary for a DH11-type device.

NOTE

Several devices have the same ranking in the SYSGEN Device Table (for example, the DMC11 and DMR11). When computing gaps, these devices should only be counted once.

A worksheet for calculating bus addresses is contained in section B.2.4. An example of calculating bus and vector addresses is contained in section B.2.5. The example should make the process clear if the explanation above did not.

B.2.3 Calculating the Interrupt Vector Address Manually

The algorithm for assigning floating vector addresses is similar to the one used for assigning bus addresses. Vector addresses are assigned in order starting at 300 and proceeding upward to 777. Table B-2 shows the assignment sequence (note that the sequence is different from the SYSGEN table used for bus addresses).

The vector address for a device is assigned on the boundary indicated in the Octal Modulus column of Table B-2. That is, if the modulus is 4, then the first vector address for that device must end with 0 or 4 (XX0, XX4); if the modulus is 10 the vector must end in 0, and so forth. The amount of space required for each device depends on the number of vectors it has. A single DHV11, for example, has two vectors, so if it were assigned an address of 300, it would also use the next legal address, 304.

Vector addresses go up sequentially and there are no gaps needed, as there are with the bus addresses. If the first device on your system were a DHV11, it would be assigned a starting vector address of 300. Its second vector would be assigned 304, so the next legal boundary for a DHV11 would be 310 (and its second vector would be assigned 314). Since no gaps are needed, the next device on your system, no matter how far down the table it was, would be assigned a vector address of 320 (unless it had a modulus that did not allow it to start at 320). The address of the device after that would depend on how many vector addresses were taken up by the device at 320.

Table B-2. Priority Ranking for Floating Vector Addresses
(footnotes at end of table)

Rank	Device	Number of Vectors	Octal Modulus
1	DC11	4	10
1	TU58	4	10
2	KL11[1]	4	10
2	DL11-A[1]	4	10
2	DL11-B[1]	4	10
2	DLV11-J[1]	16	40
2	DLV11,DLV11-F[1]	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	DM11-BB/BA	2	4
7	DH11 modem control	2	4
8	DR11-A, DRV11-B	4	10
9	DR11-C, DRV11	4	10
10	PA611 (reader+punch)	8	20
11	LPD11	4	10
12	DT07	4	10
13	DX11	4	10
14	DL11-C to DLV11-F	4	10
15	DJ11	4	10
16	DH11	4	10
17	VT40	8	20
17	VSV11	8	10
18	LPS11	12	40
19	DQ11	4	10
20	KW11-W, KWV11	4	10
21	DU11, DUV11	4	10
22	DUP11	4	10
23	DV11 + modem control	6	20
24	LK11-A	4	10
25	DWUN	4	10
26	DMC11	4	10
26	DMR11	4	10
27	DZ11/DZS11/DZV11	4	10
27	DZ32	4	10
28	KMC11	4	10
29	LPP11	4	10
30	VMV21	4	10
31	VMV31	4	10
32	VTV01	4	10
33	DWR70	4	10
34	RL11/RLV11[2]	2	4
35	TS11[2], TU80[2]	2	4

(continued on next page)

Table B-2. Priority Ranking for Floating Vector Addresses (continued)

Rank	Device	Number of Vectors	Octal Modulus
36	LPA11-K	4	10
37	IP11/IP300[2]	2	4
38	KW11-C	4	10
39	RX11[2]	2	4
39	RX211[2]	2	4
39	RXV11[2]	2	4
39	RXV21[2]	2	4
40	DR11-W	2	4
41	DR11-B[2]	2	4
42	DMP11	4	10
43	DPV11	4	10
44	ML11[3]	2	4
45	ISB11	4	10
46	DMV11	4	10
47	DEUNA[2]	2	4
48	UDA50[2]	2	4
49	DMF32	16	40
50	KMS11	6	20
51	PCL11-B	4	10
52	VS100	2	4
53	Reserved	2	4
54	KMV11	4	10
55	Reserved	4	10
56	IEX	4	10
57	**DHV11**	**4**	**10**

[1] A KL11 or DL11 used as a console, has a fixed vector.
[2] The first device of this type has a fixed vector. Any extra devices have a floating vector.
[3] ML11 is a Massbus device which can connect to a Unibus via a bus adapter.

B.2.4 System Configuration Worksheet

Figure B-3 shows a worksheet for calculating bus addresses. To calculate the bus addresses for all the devices on your system, make a list of your devices (including the DHV11s) in the order in which they appear in Table B-1 and use the following procedure:

1. Starting with the DJ11 column, mark the unit number of each DJ11 in your system in the unshaded boxes, moving downward. For example, if you had three DJ11s, you would mark a zero at 760010, a one at 760020, and a two at 760030. Skip over the shaded boxes (they represent illegal addresses). In the next legal address (760040 in this example), mark an X. (If you had no DJ11s, you would only need to mark an X in the first possible address, 760010.)

2. Now, move over one column to DH11 and assign addresses moving downward. To continue the example, in step 1 you marked an X next to address 760040 in the DJ11 column, so you would move over to the DH11 column and go down to the next legal address, 760060. If you have no DH11s in your system, you would mark an X at address 760060.

3. So far, we have used the addresses up to 760060. The next legal address in the DQ11 column is 760070. If you have no DQ11s on your system, mark an X there and move to the DU11 column.

4. Continue this process until you have assigned bus addresses to all the devices in your system. Remember that you must reserve one extra legal address (by marking an X in the box) for every possible device, even if you don't have one installed.

Calculating vector addresses is easier. Simply list all your devices in the order in which they appear in Table B-2. Do not include any devices which are not on that list. The first device has a vector address of 300 and takes up as much room as listed in the Octal Modulus column of Table B-2. For example, if you had a DC11 in your system, it would be assigned a vector of 300 and, because its modulus is 10, it takes up 10 (octal) bytes. The next device in the system would be assigned a vector of 310, unless it had a modulus that required it to start on a higher boundary.

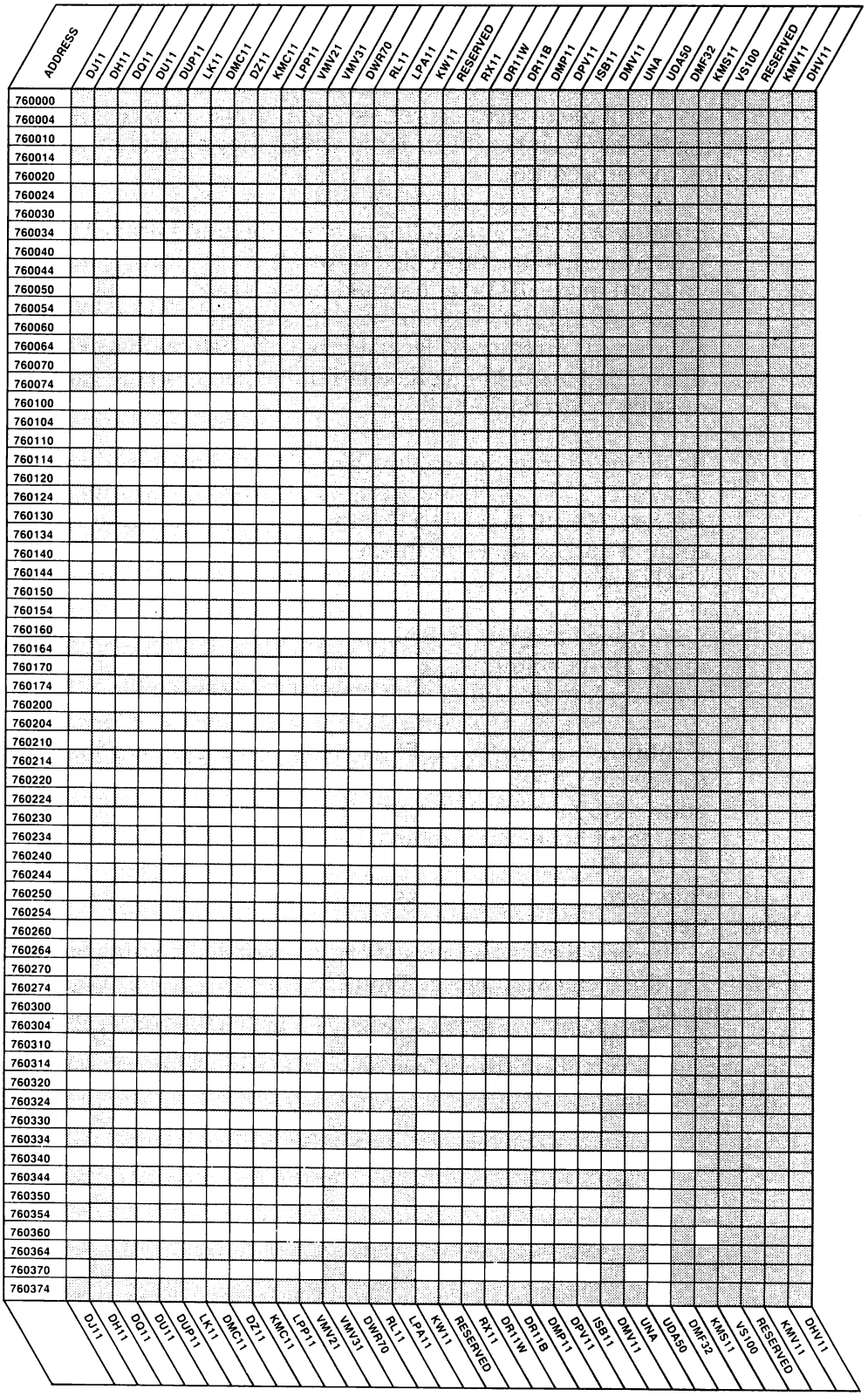
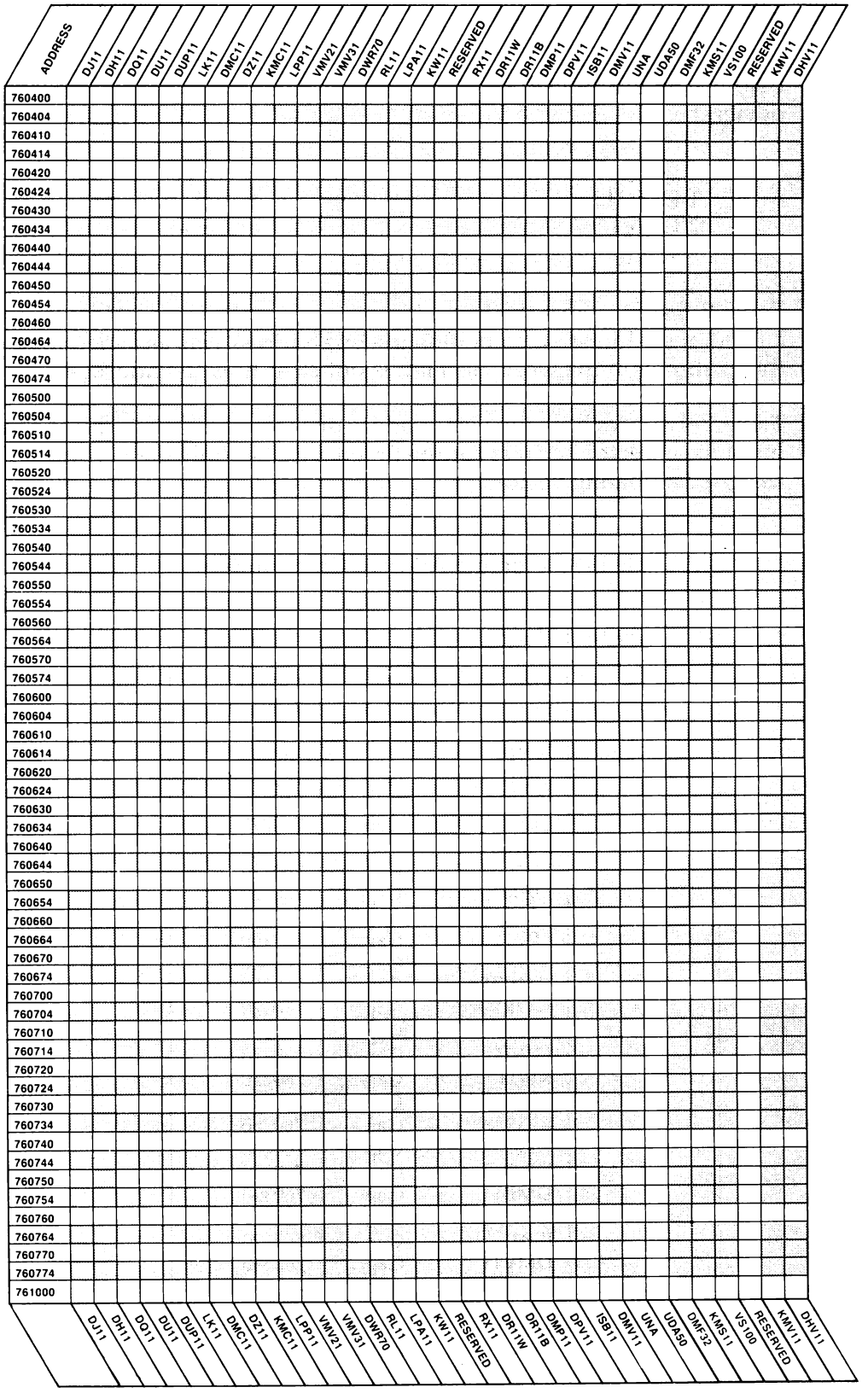


Figure B-3. Bus Address Worksheet (Page 1 of 2)



CS0801-0731B

Figure B-3. Bus Address Worksheet (Page 2 of 2)

B.2.5 A System Configuration Example

Below is an example of a system configuration which includes the following devices:

- 1 DU11
- 1 DMC11
- 2 DHV11s
- 2 TS11s

Table B-3 shows how the bus addresses were calculated. Note that the TS11 has a fixed bus addresses, so no floating bus address was assigned to it. Work out the example on the worksheet if it is not clear how the addresses were assigned.

Table B-4 shows how the vector addresses were assigned. Note that the TS11 has a fixed vector address for the first device, so only the second TS11 has been assigned a floating vector.

Table B-3. Floating Address Computation

Installed	Device		Address
	DJ11	Gap	760010
	DH11	Gap	760020
	DQ11	Gap	760030
------>	**DU11**		**760040**
	DU11	Gap	760050
	DUP11	Gap	760060
	LK11	Gap	760070
------>	**DMC11**		**760100**
	DMC11	Gap	760110
	DZ11	Gap	760120
	KMC11	Gap	760130
	LPP11	Gap	760140
	VMV21	Gap	760150
	VMV31	Gap	760160
	DWR70	Gap	760170
	RL11	Gap	760200
	LPA11	Gap	760220
	KW11	Gap	760230
	Reserved	Gap	760240
	RX11	Gap	760250
	DR11	Gap	760260
	DR11-B	Gap	760270
	DMP11	Gap	760300
	DPV11	Gap	760310
	ISB11	Gap	760320
	DMV11	Gap	760340
	DEUNA	Gap	760350
	UDA50	Gap	760360
	DMF32	Gap	760400
	KMS11	Gap	760420
	VS100	Gap	760440
	Reserved	Gap	760450
	KMV11	Gap	760460
------>	**DHV11**		**760500**
------>	**DHV11**		**760520**

Table B-4. Interrupt Vector Address Example

Device	Vector
1 DU11	300
1 DMC11	310
2 TS11s	224*
	320
2 DHV11s	330
	340

* This is the fixed vector assigned by DEC to the first TS11 in any system

Appendix C
DHV11 DIAGNOSTICS

C.1 General Description

This appendix describes the DHV11 diagnostics for LSI-11 CPUs. It includes procedures and commands for running the DHV11 diagnostic programs with the Diagnostic Runtime Services (DRS) supervisor. This appendix also contains two sample printouts of diagnostic program runs.

A different diagnostic, IQC09E, is used on MicroVAX CPUs. This diagnostic comes with its own set of documentation.

The DHV11 diagnostic programs are combined to form a Functional Verification Test (FVT) which, when run, tests various controller functions. The diagnostic programs which make up the FVT are CVDHA??, CVDHB?? and CVDHC??. The "??" at the end of the diagnostic program names indicates the revision level and patch level of the diagnostic.

NOTE

In order to run these diagnostics without error, you must disable the Emulex options in the CS08/E1 configuration program. See section 4.4 for details.

The minimum system requirements to use the DHV11 diagnostic programs are:

- LSI-11 Bus CPU
- 32K bytes of memory
- Console terminal
- XXDP+ load device with Diagnostic Runtime Services supervisor
- CS08/E1 Communications Subsystem

In order to test the full DMA address capability of the controller, the FVT uses the following address patterns. If the high address lines are to be tested, the host must have addressable memory at the following locations as well as the 32K bytes defined above:

Address Bits	21	20	19	18	17	16	15	14	13	-	-
Memory Address (High bank)	1	0	1	0	1	0	1	X	X	X	X
Memory Address (Low bank)	0	1	0	1	0	1	0	X	X	X	X

If memory is not available at these locations some high DMA address bits will not be tested. This will not be considered as an error. The operator, by answering a prompt, can display information specifying the bits that were tested.

NOTE

Diagnostics CVDHB?? and CVDHC?? can optionally use either wrap-around connectors or staggered loopback cables. Schematics for these connectors and cables can be found in the distribution panel technical manual. If staggered loopback cables are used, they must be installed as shown in Figure C-1.

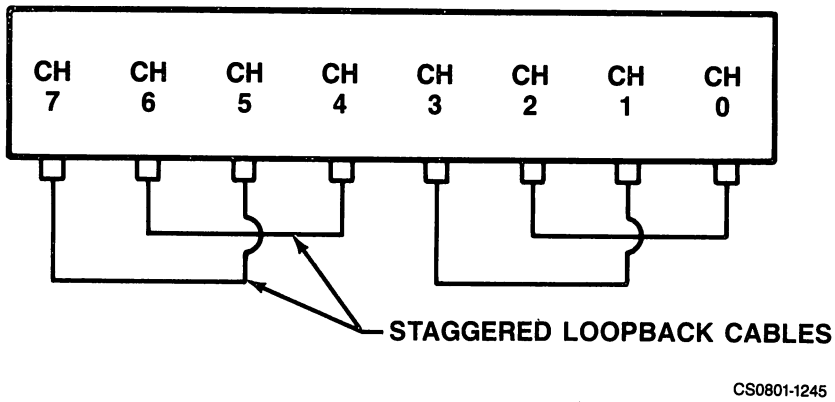


Figure C-1. Staggered Loopback Cable Configuration

C.2 Diagnostic Test Functions

CVDHA??

This program checks the reset and the register access functions, and verifies that the handshake between the controller and the host is operating correctly. It also checks reports from the self-test. This diagnostic test does not require the use of wrap-around connectors.

CVDHB??

This program checks the major communication functions of the controller. It verifies correct operation of modem control signals and the register bits which control and report them. This diagnostic does not perform extensive data transmission and reception tests. The diagnostic queries for the type of loopback being used: external wrap-around connectors (H325) or staggered loopback cables (H3277). If internal loopback is chosen, the RS-232-C drivers and receivers are not tested.

CVDHC??

This diagnostic checks the major communications functions which use the DUARTs. It checks split-speed operation, and verifies that DUART errors are reported correctly. Extensive data transfer tests are performed in both DMA and single-character modes. The diagnostic queries for the type of loopback being used: external wrap-around connectors (H325) or staggered loopback cables (H3277). If internal loopback is chosen, the RS-232-C drivers and receivers are not tested.

C.2.1 Diagnostic Exceptions

CVDHC?? may fail tests 8 and 9 when running XXDP+ with the extended monitor. This is caused by the higher performance of the CS08/E1 compared to the DEC DHV11. These tests pass if the nonextended monitor is used.

CVDHB?? tests modem control signals. If the modem control board (attached to the rear of the CP08/M Distribution Panel) is missing, or if you are using a CP08/J, tests 16 through 21 will fail if external loopback or staggered loopback is selected.

C.3 Diagnostic Supervisor Summary

The DHV11 diagnostics have been written for use with the Diagnostic Runtime Services (DRS) supervisor. DRS, which provides the interface between the operator and the diagnostic programs, can be used with load systems such as ACT, APT, SLIDE, XXDP+, and ABS loader. By answering prompt questions supplied by the supervisor the operator can define the following:

- The hardware configuration of the controllers being tested
- The type of test information to be reported
- The conditions under which the test should be terminated or continued.

C.4 Loading Procedures

There are several different methods for loading the DHV11 diagnostics under the control of the XXDP+ diagnostic monitor. The following procedure is common to many DEC systems and similar to others.

1. Mount the appropriate medium (Dectape, disk, etc.) containing the XXDP+ monitor and the Functional Verification Test.

2. Boot the system to load the monitor.

3. Once loaded, the XXDP+ monitor prints an introductory message and displays a period (.) to indicate that it is ready to accept commands.

4. To display a list of the diagnostic programs contained on the tape (or disk), type DIR at a period prompt.

5. The diagnostic may now be loaded. There are two different ways to load the diagnostic. The two methods are described below. The diagnostic CVDHAB0 (where the B0 at the end of the name indicates the revision level and the patch level of the diagnostic) is used as an example in both of the methods.

   a. To load the diagnostic CVDHAB0, type:

      L CVDHAB0

      The DRS supervisor can now be started. At the prompt, type:

      S 200

   b. To load the diagnostic and start the DRS supervisor with a single command, type:

      R CVDHAB0

6. The diagnostic and the DRS supervisor will be loaded. The following message is then displayed:

```
DRS LOADED
DIAG. RUN-TIME SERVICES REV. D APR-79
CVDHAB0
DHV-11 FUNC TST PART1
UNIT IS DHV-11
DR>
```

DR> is the prompt for the DRS supervisor routine. At this point a DRS supervisor command (such as START) must be entered. The DRS supervisor commands are listed in subsection C.6.

C.5 Starting the Diagnostic Program

Use the DRS Supervisor to start the diagnostic program. The start procedure has four steps. The start command is issued, hardware parameter questions are answered, software parameter questions are answered, and the diagnostic is executed. These steps are presented in greater detail below.

1. At the prompt DR> type:

   STA/PASS:1/FLAGS:HOE<CR>

   The switches and flags are optional.

2. The program prompts with:

   CHANGE HW?

   You must answer Y to this prompt to change the hardware parameter tables.

   NOTES

   Some versions of the diagnostic supervisor do not ask if you would like to alter the hardware parameter tables. Instead, they begin with the hardware parameter question sequence.

   When running diagnostic programs CVDHB?? and CVDHC??, be sure to set the BR level to the value selected in the CS08/E1 configuration program. The standard setting is BR4. The BR level may be set when changing the hardware parameter tables.

   The answers to the hardware questions are used to build hardware parameter tables in memory. A series of questions is presented for each device to be tested, and a table is built for each device.

3. When all of the hardware parameter tables have been built, the program presents the prompt for the software parameter tables. This prompt is as follows:

   CHANGE SW?

   If parameters other than the default parameters are desired, type Y. If you wish to use the default parameters, type N.

   If you type Y, a series of questions will be asked which prompt you to enter desired software parameters. These parameters will be entered in the software parameter table in memory. Unlike the hardware questions, the software questions will be asked only once, regardless of the number of units being tested.

4. After the software parameter tables have been built, the diagnostic begins to run.

   The program printouts and actions on error detection are determined by the switch options selected with the start command.

C.6 DRS Supervisor Commands

The following DRS supervisor commands may be issued in response to the DR> prompt:

COMMAND	FUNCTION
START	Starts a diagnostic program
RESTART	When a diagnostic has stopped and control is returned to the supervisor, this command restarts the program from the beginning
CONTINUE	Allows a diagnostic to continue running from the point where it was stopping point
PROCEED	Causes the diagnostic to resume with the next test after the one it halted in
EXIT	Transfers control to the XXDP+ monitor
DROP	Drops units specified until an ADD or START command is given
ADD	Adds specified units. These units must have been previously dropped
PRINT	Prints out statistics if available
FLAGS	Used to change flags
ZFLAGS	Clears flags

All of the DRS supervisor commands except EXIT, PRINT, FLAGS and ZFLAGS can be used with switch options.

C.6.1 Command Switches

Switch options may be used with most DRS supervisor commands. The commands and their functions and some examples are listed below.

COMMAND	FUNCTION
/TESTS:	Used to specify the tests to be run (the default is all tests). An example of the tests switch used with the start command to run tests 1 to 10, 20 and 30 to 35 would be: DR> START/TESTS:1-10:20:30-35<CR>
/PASS:	Used to specify the number of passes for the diagnostic to run. An example of the tests switch used with the start command to make two passes would be: DR> START/PASS:2
/EOP:	Used to specify how many passes of the diagnostic will occur before the end of pass message is printed (the default is one). An example of the tests switch used with the start command to prompt the program to report the end of a pass after every third pass would be: DR> START/EOP:3
/UNITS:	Used to specify the units to be run. This switch is valid only if N was entered in response to the CHANGE HW? question.
/FLAGS:	Used to check for conditions and modify program execution accordingly. It is possible to enable multiple flags at the same time. An example of the format to do this is as follows: DR> START/FLAGS:HOE:PNT The conditions checked for are as follows: :HOE Halt on error (transfers control back to the supervisor) :LOE Loop on error :IER Inhibit error reports :IBE Inhibit basic error information :IXE Inhibit extended error information :PRI Print errors on line printer :PNT Print the number of the test being executed befor execution :BOE Ring bell on error :UAM Run in unattended mode, bypass manual intervention tests :ISR Inhibit statistical reports :IDU Inhibit dropping of units by program

C.6.2 Control/Escape Characters Supported

The keyboard functions supported by the DRS supervisor are as follows:

COMMAND	FUNCTION
CTRL C	Returns control to the supervisor. The DR> prompt would be typed in response to CTRL C. This command can be typed at any time.
CTRL Z	Used during hardware or software dialogue to terminate the dialogue and select default values.
CTRL O	Disables all printouts. This is valid only during a printout.
CTRL S	Used during a printout to temporarily freeze the printout.
CTRL Q	Resumes a printout after a CTRL S.

C.7 DHV11 Diagnostic Example

This subsection contains a sample printout of CVDHBC0. The program is loaded and the DRS supervisor is started with a RUN command. This example depicts an error free pass.

The example begins after the operating system has been booted. The XXDP+ operating system uses . as a prompt. The DRS supervisor routine uses DR> as a prompt.

Entries made by the operator are underlined. The symbol <CR> represents a carriage return.

Example C-1.

```
.R CVDHBC0<CR>
CVDHBC0.BIC

DRS
CVDHC-C-0
DHV-11 FUNC TST PART2
UNIT IS DHV-11
RESTART ADDR: 147670
DR>STA

CHANGE HW (L) ? Y<CR>

# UNITS (D) ? 1<CR>

UNIT 0
CSR ADDRESS: (0) 160460 ? <CR>
INTERRUPT VECTOR ADDRESS (0) 300 ? 320<CR>
ACTIVE LINE BIT MAP: (0) 377 ? <CR>
TYPE OF LOOPBACK (1=INTERNAL, 2=H3277, 3=H325): (0) 2 ?
1<CR>
INTERRUPT BR LEVEL: (0) 4? <CR>

CHANGE SW (L) ? Y<CR>

REPORT UNIT NUMBER AS EACH UNIT IS TESTED:(L) Y ? <CR>
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE:
(D) 0 ? 1<CR>

TESTING UNIT: 0 (D)

CVDHB EOP   1
0 CUMULATIVE ERRORS

TESTING UNIT : 0(D)
<control-c>
DR>EXIT
```

Appendix D
PROM REMOVAL AND REPLACEMENT

D.1 Overview

It may be necessary, either for maintenance or upgrade reasons, to remove and replace the CC08's emulation PROM set.

The CS08/E1 contains the following six emulation PROMs:

- G26
- G27
- G28
- G29
- G30
- G31

The CS08/E1 also contains a Message PROM that may be upgraded in the field. It has the following number:

- G32

Figure D-1 shows the locations of the PROMs on the PCBA. Pry the existing PROMs from their sockets using an IC puller or equivalent tool.

The new emulation PROMs must be placed in their sockets in the correct order. Place the lowest numbered emulation PROM in the socket labeled "0" in Figure D-1, the next in the socket labeled "1," and so forth.

Make sure that the PROMs are firmly seated and that no pins are bent or misaligned. If the two rows of pins are too far apart to fit in the socket, bend one row of pins inward by pressing it against a table top or other flat surface.

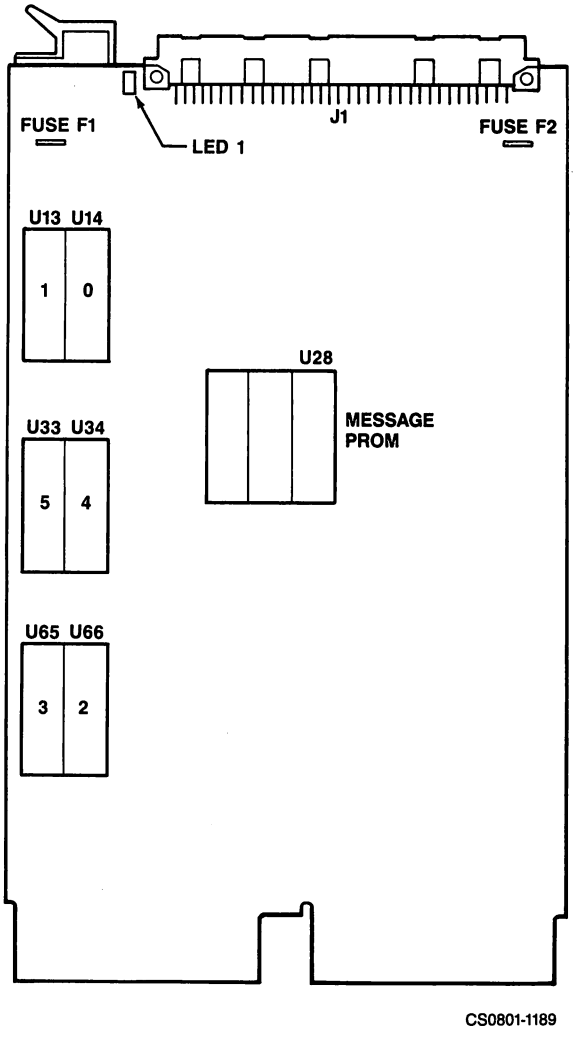


Figure D-1. Location of CS08/E1 Emulation PROMs on PCBA

Appendix E
ASCII CODE CONVERSION

Octal	Hex	Dec	Mnemonic	Description	Octal	Hex	Dec	Mnemonic	Description
000	00	000	NUL	Blank	100	40	064	@	
001	01	001	SOH	Start of Header	101	41	065	A	
002	02	002	STX	Start of Text	102	42	066	B	
003	03	003	ETX	End of Text	103	43	067	C	
004	04	004	EOT	End of Transmission	104	44	068	D	
005	05	005	ENQ	Enquiry	105	45	069	E	
006	06	006	ACK	Acknowledge (Positive)	106	46	070	F	
007	07	007	BEL	Bell	107	47	071	G	
010	08	008	BS	Backspace	110	48	072	H	
011	09	009	HT	Hoizontal Tab	111	49	073	I	
012	0A	010	LF	Line Feed	112	4A	074	J	
013	0B	011	VT	Vertical Tab	113	4B	075	K	
014	0C	012	FF	Form Feed	114	4C	076	L	
015	0D	013	CR	Carriage Retrun	115	4D	077	M	
016	0E	014	SO	Shift Out	116	4E	078	N	
017	0F	015	SI	Shift In	117	4F	079	O	
020	10	016	DLE	Data Link Escape	120	50	080	P	
021	11	017	DC1	Device Control 1 (XON)	121	51	081	Q	
022	12	018	DC2	Device Control 2	122	52	082	R	
023	13	019	DC3	Device Control 3 (XOFF)	123	53	083	S	
024	14	020	DC4	Device Control 4 - Stop	124	54	084	T	
025	15	021	NAK	Acknowledge (Negative)	125	55	085	U	
026	16	022	SYN	Synchronization	126	56	086	V	
027	17	023	ETB	End of Text Block	127	57	087	W	
030	18	024	CAN	Cancel	130	58	088	X	
031	19	025	EM	End of Medium	131	59	089	Y	
032	1A	026	SUB	Substitute	132	5A	090	Z	
033	1B	027	ESC	Escape	133	5B	091	[	Opening Bracket
034	1C	028	FS	File Separator	134	5C	092	\	Reverse Slash
035	1D	029	GS	Group Separator	135	5D	093	]	Closing Bracket
036	1E	030	RS	Record Separator	136	5E	094	^	Circumflex
037	1F	031	US	Unit Separator	137	5F	095	_	Underline
040	20	032	SP	Space	140	60	096	`	Opening Single Quote
041	21	033	!		141	61	097	a	
042	22	034	"		142	62	098	b	
043	23	035	#		143	63	099	c	
044	24	036	$		144	64	100	d	
045	25	037	%		145	65	101	e	
046	26	038	&		146	66	102	f	
047	27	039	'	Closing Single Quote	147	67	103	g	
050	28	040	(		150	68	104	h	
051	29	041	)		151	69	105	i	
052	2A	042	*		152	6A	106	j	
053	2B	043	+		153	6B	107	k	
054	2C	044	,	Comma	154	6C	108	l	
055	2D	045	-	Hyphen	155	6D	109	m	
056	2E	046	.	Period	156	6E	110	n	
057	2F	047	/		157	6F	111	o	
060	30	048	0		160	70	112	p	
061	31	049	1		161	71	113	q	
062	32	050	2		162	72	114	r	
063	33	051	3		163	73	115	s	
064	34	052	4		164	74	116	t	
065	35	053	5		165	75	117	u	
066	36	054	6		166	76	118	v	
067	37	055	7		167	77	119	w	
070	38	056	8		170	78	120	x	
071	39	057	9		171	79	121	y	
072	3A	058	:		172	7A	122	z	
073	3B	059	;		173	7B	123	{	Opening Brace
074	3C	060	<	Less Than	174	7C	124	|	Vertical Line
075	3D	061	=		175	7D	125	}	Closing Brace
076	3E	062	>	Greater Than	176	7E	126	~	Overline (Tilde)
077	3F	063	?		177	7F	127	DEL	Delete/Rubout

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